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ADVANCED MAIL SYSTEMS SCANNER TECHNOLOGY. EXECUTIVE SUMMARY AND--ETC(U)
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THIRD ANNUAL REPORT
ADVANCED MAIL SYSTEMS SCANNER TECHNOLOGY

Executive Summary and Appendixes A-D

October 1977

Prepared by
NOSC Sensor Processing and Analysis Division (Code 732)
NAVAL OCEAN SYSTEMS CENTER
San Diego, California 92152

FOR
US POSTAL SERVICE
OFFICE OF ADVANCED MAIL SYSTEMS DEVELOPMENT

AMSD

NAVAL OCEAN SYSTEMS CENTER, SAN DIEGO, CA 92152

AN ACTIVITY OF THE NAVAL MATERIAL COMMAND

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ADMINISTRATIVE INFORMATION

This report contains a summary of work sponsored by the Office of Advanced Mail Systems Development, Research and Development Department of the US Postal Service, Rockville, Maryland 20852, under US Postal Service Agreement 104230-76-T-0798. The authorized USPS technical representative is Victor P. Boyd. The principal NOSC investigator is Frank C Martin of the Signal Analysis and Image Processing Branch, NOSC Code 7323. Associate investigators are Thomas R Little, Clinton V Mayo, and Lee A Wise, also of Code 7323. Other contributors include Joseph M Greene and Waldo R Robinson of Code 8235, A Duane Gomez of Code 8246, and Robert W Basinger, student/contractor. This report is a compilation of data presented by all team members and was approved for publication in October 1977.

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The objective of the effort described herein is to provide technical consultation, equipment, and support services to the US Postal Service which will contribute to the development of the system definition of a new-concept processing system, the Electronic Message Service (EMS). Included in the scope of effort are investigations of high-speed image scanning technology, image frame memory storage, image enhancement, and the fabrication of a scanner/frame-store memory test assembly.

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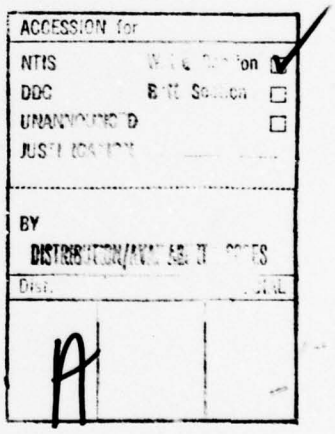

OBJECTIVES

1. Provide the US Postal Service the technical consultation, equipment, and support services which will contribute to the development of the system definition of a new-concept processing system, the Electronic Message Service (EMS). Include in this scope of effort (1) investigations in scanner technology, image frame memory storage, and image enhancement, and (2) the design and fabrication of a scanner/frame-store memory test assembly.

2. Contribute to the selection of the most optimum imaging devices and techniques for high-speed image acquisition. Provide reliable designs of high-speed image processing logic which will preserve the quality of the image while reducing the image storage and transmission requirements and minimizing vulnerability of the image information to noise during processing, transmission, and reproduction.

3. Act as technical consultants to the USPS Office of Advanced Mail Systems Development in preparing technical requirements and statements of work and evaluating technical proposals and contractor performance; and perform technical evaluation of contractor-produced developmental equipment.

RESULTS

1. Selection and procurement of equipments and components required for a major upgrading of the Image Capture and Analysis System (ICAS) have been completed.

2. A significant number of these equipments which were obtained to replace GFE items have been interfaced and are operating.

3. The remaining major items have been fabricated and are in the process of being debugged and installed at this time.

4. Modifications to the large drum test bed (LDTB) have been made to accommodate variable resolution imaging studies.

5. Test and evaluation of imagers continued.

6. New circuitry has been designed to drive the new imagers. The new input design includes remote control of wideband gain and level circuits, new clock drivers, and very high-speed analog-to-digital converters.

7. The addition of the Tektronix model 4051 terminal has added significantly to the control and data handling capability of the ICAS.

8. One interface of the Versatec model 1200A line printer/plotter is now complete, allowing all image statistical data and processing programs to be documented in high-quality hard-copy form.

9. Four technical reports were submitted to AMSD in the reporting period. They are included here as appendixes.

10. A contract issued to RCA Princeton for the development of a time-delay-integration (TDI) imager was completed. Operation of a TDI imager having characteristics which can meet all the USPS imaging goals has been demonstrated. A second contract to refine and expand the approach is under consideration at this time.

PLANNED FUTURE NOSC ACTIVITIES

1. Complete the interface debugging of the new equipments in the ICAS.

2. Study and refine the data path from imager through the digitization process. This will include the illumination correction process.

3. Expand the data base of document characterization to determine the parameters best suited for selection of illumination, enhancement, compression, and storage techniques.

4. Operate the RCA TDI imager in the LDTB at the maximum speed possible in order to provide feedback for imager and driver electronics design improvements.

5. Refine the NOSC "meander" compression algorithm and attempt to optimize the patterns for various image types.

6. Follow up on promising previous year's study by performing new experiments on logarithmic video compression.

7. Obtain and evaluate any new imagers that emerge during the year which appear to be suitable for Postal Service use.

CONTENTS

ILLUSTRATION

GLOSSARY

ac	Alternating current
A/D	Analog to digital
address	Peripheral device selection or memory location specification
ALU	Arithmetic/logic unit
AMSD	Office of Advanced Mail Systems Development
ASCII	American Standard Code for Information Interchange
baud	Effective bit rate in bits per second
bit	The smallest piece of digital information – either 0 or 1
bit serial	The bits of a character are transmitted serially
bootstrap	A built-in function which eases system start-up
byte	A logical group of bits (8 is standard)
CCD	Charge-coupled device
CCPD	Charge-coupled photodiode
CPE	Central processing element
CPU	Central processing unit
CTF	Contrast transfer function
D/A	Digital to analog
dc	Direct current
DIA	Digital Image Analyzer
DMA	Direct memory access
DPCM	Differential pulse code modulation
EAROM	Electrically alterable read-only memory
ECL	Emitter-coupled logic
EDM	Engineering development model
EMSS	Electronic Message Service System
FCU	Format Control Unit
FDS	First difference statistics
FET	Field-effect transistor
Fetch	Microroutine which retrieves MCU instructions from program memory
file	On magnetic tape, a grouping of logical records
filemark	A logical gap between tape files
firmware	System control by use of ROMs and a microprogram sequencer
fpf bit	Front-panel fetch bit; indicates that MCU instruction is from front panel
FSM	Frame-Store Memory
GFE	Government furnished equipment
GPIB	IEEE STD 488-1975 General-Purpose Interface Bus for asynchronous data communications

Gray code	A binary code in which only one bit changes at each increment
HCU	Hard-copy unit
HIC	Hardware Illumination Corrector
Hz	Hertz; cycles per second
ICAS	Image Capture and Analysis System
IEEE	Institute of Electrical and Electronics Engineers
interrecord gap	Physical space between magnetic tape logical records
I/O	Input/output
k	1024
kW	Kilowatts
LDTB	Large Drum Test Bed
LED	Light-emitting diode
LFPM	Linear feet per minute
listener	A device which may receive data on the GPIB
logical record	A logical grouping of data on magnetic tape. In an image, a video line is treated as a logical record
LSI	Large-scale integration
M	Mega-; million
machine language	Operation instructions interpretable by the machine being operated
macroinstruction	A machine language instruction which initiates a sequence of basic machine operations
macrolevel	A level at which an operator may directly communicate with a machine; ie, machine language level
macroprogram	A logical sequence of macroinstructions
MARB	Memory Address Register Bus
MCU	Memory Control Unit
message	On the GPIB, a sequence of data and/or control operations transmitted
MIC	Memory Interface Card
MICC	Memory Interface Control Card
microaddress	Micromemory address
microcode	Bit-by-bit implementation of microinstructions
microcontrol	Control of individual hardware resources by use of a microprogram structure
microinstruction	A basic machine operation instruction containing control for all hardware resources (eg, data paths, registers, ALUs)
microlevel	Hardware direct-control level
micromemory	Memory (usually ROM) which contains micro-instructions
micromemory address	Specification of location within a micromemory

microprogram	A logical sequence of microinstructions
microroutine	A microprogram or part thereof
MIU	Memory Interface Unit
MOS	Metal oxide semiconductor
MSB	Most significant bit
MTBF	Mean time between failures
MTF	Modulation transfer function
n	Multiplex ratio
NELC	Naval Electronics Laboratory Center
nm	Nanometre
NOSC	Naval Ocean Systems Center
ns	Nanosecond
NTC	National Telecommunications Conference
page	An 8½-by-11-inch acquired image or original copy
PBS	Pel brightness statistics
PC	Personality Chassis
PCR	Print contrast ratio $=(r_{max} - r_{min})/r_{max}$
pel	Picture element
Pixel	Picture element
PPHE	Printer and paper-handling equipment
PPHE/IU	Printer and paper-handling equipment/input unit
PPE	Printer/plotter equipment
program	Macro program
PROM	Programmable read-only memory
r	Reflectivity
RAC	Relative address coding
RALU	Register arithmetic logic unit
RAM	Random-access (read/write) memory
record	Logical record
RLC	Run length coding
RLS	Run length statistics
ROM	Read-only memory
SDC	Systems Development Corporation
SDTB	Small Drum Test Bed
s	Second
SID	Silicon imaging device
SPADE	Storage, Processing, and Display Equipment
SPIE	Society of Photo-Optical Instrumentation Engineers
t_{mac}	Memory access time
t_{mcy}	Memory cycle time
talker	A device which may transmit asynchronous data on the GPIB
TDI	Time-delay integration

TDMA	Time-division multiple access
three-wire handshake	The Hewlett-Packard patented method of guaranteeing asynchronous communication capability on the GPIB
TTL	Transistor-transistor logic
USPS	United States Postal Service
UV	Ultraviolet
VTS	Video transmission system (Navy)
word	A grouping of 1 or more bytes (in the MCU, a word contains 6 bytes, or 48 bits)

RELEVANCE TO DoD MISSION

The concept definition phase of the Electronic Message Service System (EMSS) is nearing completion, and selected alternatives will soon be forthcoming, which the USPS will evaluate to select a proposed system approach. If instrumented, it will become the second largest communication and information exchange system in the US. Participation on the imaging interface aspects of the system provides intimate familiarity for the Navy, which will be able to assist in utilization of the network for military purposes in a time of national need.

The actual imaging investigation is relevant to recent and current NOSC programs involving facsimile and submarine sensors. One of the requirements of the Tactical Flag Command Center program is image transmission. Other requirements for image acquisition, processing, storage, and transmission are implicated in work for the Naval Intelligence Support Center. The USPS Image Capture and Analysis System (ICAS) has been designed to interchange data with the NOSC video test bed in the Display Equipment Development Branch, Code 8247. Digital image tapes can be generated by scanning or by converting tapes from other sources to a format compatible with the Laser Recording System located in the Marine Corps and Special Systems Branch, Code 8125.

One of the program procurements is a large, high-speed imaging, charge-coupled device (CCD) which can operate in the time-delay-integration (TDI) mode. This single device is capable of acquiring full-page data at a rate of 20 pages per second. The high performance of the device makes it applicable for telereconnaissance, teleguidance, battlefield surveillance, and intrusion detection as well as document imaging. Successful operation of the device has been witnessed at the contractor's facility, and negotiations are being considered for refinement and advancement of this important work.

The experience gained with microprocessor architecture, image processing, high-speed storage and retrieval, display, and hard-copy generation is also valuable to the Navy. Very little of the work within the DoD and academic communities involves high-speed, real-time hardware and algorithm developments which will support military applications such as:

- ocean surveillance
- telereconnaissance
- teleguidance
- battlefield surveillance
- intrusion detection
- image transmission systems
- pattern/character recognition
- word processing

EMS GOALS

The USPS has undertaken the investigation of advanced mail systems. An important element in this program is the investigation of a possible Electronic Message Service (EMS). The USPS is conducting a detailed system definition effort for the purpose of establishing the technical and economic feasibility of a nationwide EMS concept. Functionally, EMS would accept messages in digital or paper copy form, convert inputs, as required, into digital form, transport message inputs electronically from source to EMS destination over communication networks, and either convert the message back to paper copy form for carrier delivery to the recipient or deliver it to the customer by alternative electronic delivery systems.

The phrase "paper copy form" can imply many formats such as typed, drawn, or handwritten information of various colors on paper of almost any color and continuous-tone pictures that may be in black and white or many colors. The Office of Advanced Mail Systems Development (AMSD) has determined in this initial analysis that it will ultimately be necessary to scan page-like material with these criteria:

1. The data can be in typed, printed, handwritten, or continuous-tone form.
2. The text data can be most colors on most colors of paper.
3. The continuous-tone data can be black and white or multicolor.
4. The scanning technique must be capable of at least 80 lines per centimetre (200 lines per inch).
5. Within the limits of system resolution, the quality of the reproduced transmitted message must be very nearly equal to that of the original.

In addition to the above input criteria, AMSD has determined that the material may be required to be scanned at a rate equivalent to twenty 8½-by-11-inch pages per second in order to handle the volume anticipated for an EMS system. As a point of comparison, messages currently sent by facsimile are handled at a rate of 4800 bits per second. At this bit rate it would take facsimile transmission equipment 78 minutes to transmit a black and white image with anticipated EMS quality.

The concept of EMS remains unchanged from what was discussed in last year's annual report.

NOSC MISSION

The large disparity between existing scanning technology and the goals of the envisioned EMS required the implementation of a major development program. In October 1974 the USPS and NELC signed an agreement in which NELC, primarily the Display Division, agreed to provide technical support for 1 year for the development of scanning technology for the very advanced EMS system. Acceptable progress during 1975 resulted in the issuance of a second agreement for work to begin in October 1975. A third agreement was issued covering the period from October 1976 to October 1977. Annual reports were written to summarize the first two years' accomplishments.* This

*First Annual Report Advanced Mail Systems Scanner Technology, 22 October 1975, prepared by NELC Display Division, NELC TR 1965.
Second Annual Report Advanced Mail Systems Scanner Technology, October 1976, prepared by NELC Display Division, NELC TR 2020.

report covers the third year's work beginning 9 October 1976 and ending 8 October 1977.

Tasks performed and services provided by NELC/NOSC during these 3 years have included:

1. Survey of available imaging devices and technologies and comparative analysis of capabilities
2. Characterization of imaging devices with respect to dynamic range, sensitivity, and spectral response
3. Characterization of various illumination sources and techniques
4. Design and construction of a test bed for use in demonstrating and evaluating hardware, software, and techniques for image scanning at the specified rates
5. Investigation of video compression, image enhancement, and data compression techniques
6. Generation of high-quality test images that are stored on tape; enhancement of data and comparison of results with original images
7. Development of illumination correction techniques
8. Evaluation of lenses for use in image scanning
9. Evaluation of adaptive thresholding
10. Study of effects of scan density on image quality
11. Compilation of technical reports on specific aspects of the work as well as progress and year-end summary reports
12. Consultation and support services including the monitoring of hardware contracts, evaluation of proposals, and writing of procurement specifications

1975 HIGHLIGHTS

Some significant accomplishments of the year ending 21 October 1975 included:

1. A 12-inch-circumference drum scanner/frame-store memory test bed was designed, fabricated, and operated.
2. Promising newly available large high-speed imagers were procured and successfully evaluated. (Previously it appeared that several smaller solid-state imagers mounted on a very critical optical mixing device would be required to scan a full page width.)
3. The investigations into edge and image enhancement techniques were begun. In conjunction with these efforts it was determined that a prestorage image analyzer could be used. The analyzer was designed, fabricated, and successfully operated.
4. Methods of achieving nonlinear video amplitude partitioning and of establishing dynamic range and automatic threshold detection were studied, and designs for later installation in the scanner/frame-store memory test bed were completed.

1976 HIGHLIGHTS

Some significant accomplishments of the year ending 8 October 1976 include:

1. A 40.92-inch-circumference large drum test bed (LDTB) was designed and fabricated, compatible with Pitney Bowes paper-handling equipment.

2. High-brightness fluorescent lamps were evaluated for use in the LDTB and found to be superior, for this application, to the quartz halogen lamp used in the small drum test bed that was developed during the previous year.

3. Software was developed to compensate for nonuniform illumination.

4. Special fluorescent lamps were procured in which the mixture of phosphors compensates for fall-off in imager sensitivity from red to blue.

5. Test and evaluation of imagers continued. The ranking of the contenders changed as the result of the emergence of new and improved devices.

6. New CCD driver boards incorporating best available high-speed logic techniques were designed and fabricated.

7. Image analyzer capability was expanded so that first difference and run length statistics may be provided in addition to the original pel brightness statistics.

8. Progress was recorded throughout the software hierarchy running from microcodes up to high-level procedural programs. Corresponding hardware improvements were effected. High-speed PROMs incorporating microcode data, for example, replaced the low-speed PROMs previously used in the memory controller.

9. Six technical reports were submitted to AMSD in the reporting period.

10. A contract was issued to RCA Princeton for the development of a tracking/time-delay-integration imager.

1977 TASKS

For the year ending 9 October 1977, the services performed can be divided into five categories. The categories and tasks within each are listed below.

Hardware deliverables

- Select and procure ICAS system upgrade equipments
- Replace GFE items with USPS equivalents
- Add extended semiconductor memory and interface
- Add "personality unit" to ICAS
- Add remotely controlled gain/level circuits
- Modify LDTB for variable-resolution tests
- Initiate TDI tests

Software deliverables

- Generate extensive terminal programs
- Generate image processing routines

Digitally simulate analog adaptive threshold

Generate meander compression analysis routines

Program image tape format conversions

Documentation deliverables

ICAS third report

Resolution study report

Advanced prestorage processing report

Data compression summary report

Major procurement contracts

Imager for time delay integration (TDI) with RCA, Princeton Laboratories

Support services

Resolution test, 60 image tapes

Subjective lens/copy orientation test

Design review technical support

Some of the categories of effort involved considerable overlap – notably hardware, software, and documentation. In the next section of this executive summary the first two categories of tasks are described in detail. The material presented for the third category, documentation deliverables, will be essentially the results and/or conclusions from each document, because each is included in its entirety as an appendix. The fifth category, support services, is not detailed further.

1978 PLANS

The plans for FY78 will follow much the same format as those for FY77. The categories of work and the tasks within each are listed below.

Hardware deliverables and imaging studies

Complete the interface debugging of the new equipments in ICAS.

Obtain and evaluate any new imagers which appear during the year that may be suitable for Postal Service use.

Study and refine the image data path from the imager through the digitization process, including illumination correction.

Operate the RCA TDI imager in the LDTB at the maximum speed possible in order to provide feedback for imager and driver electronics design improvements.

Refine the NOSC "meander" compression algorithm and attempt to optimize the patterns for various image types.

Follow up on promising previous year's study by performing new experiments on logarithmic video compression.

Investigate techniques to optically compensate for the majority of illumination nonuniformity.

Generate characterization data on the sets of data types to be scanned.

Investigate requirements for, and assist in procurement of, if needed, a precision flat bed scanner to be added to the ICAS.

Study the possibility of programmable variable resolution.

Software deliverables

Add program routines to control remote gain and level circuits.

Study algorithms which offer promise to sort documents into classes, bilevel (black/white only) or continuous tone (photographic).

Develop programs for control of other interfaces such as the digital image analyzer (DIA) and the printer.

Documentation deliverables

Data capture interim report

TDI imager interim report

EDM hardware evaluation report

Advanced compressibility report

Interim color imaging report

Monthly progress/technical reports

Fourth annual report of total program

Specification for flat bed mechanism

Major procurement contracts

Continue development of the tracking TDI imager.

Support services

Provide technical liaison support between various vendors and AMSD.

Provide technical consultation to AMSD as requested.

TASK SUMMARIES

HARDWARE

GFE EQUIPMENT REPLACEMENT

To alleviate potential schedule impacts which might have been caused to Navy or USPS programs, a number of equipments were purchased from program funds to replace all GFE components.

A Tektronix model 4051 terminal was procured and installed to replace the GFE Tektronix model 4023 terminal. A Versatec model 1200A printer/plotter was added to the ICAS to replace the GFE Tektronix model 4632 hard-copy unit. The GFE Conrac RQB 14-inch monitor display was replaced with an identical unit which is program property. A second Kennedy model 9000 tape deck was added to replace the GFE Bright model BI 2600 unit.

ICAS SYSTEM UPGRADE

In order to prepare for high-speed image acquisition from the RCA time-delay-integration (TDI) four-ported imager, four new Phoenix Data analog-to-digital (A/D) converters were procured. Three of these units are model 1106-60 which operate at 60 million conversions per second. The fourth is a model 1106-100 which operates at 100 million conversions per second. These units replace the simple Datel model SHM-UH sample-and-hold unit and the model ADC-UH6B A/D converter.

Seven new 65 k-word by 48-bit model 300-0000-001 Monolithic Systems memory units were added to the ICAS. These memories, of which six were purchased by USPS and shipped to NOSC and one was obtained on program funds, are identical to the original memory unit already operating. The total capacity, approximately 25 million bits, provides for the acquisition of a full 8½-by-11-inch image at 200 by 200 pels per inch at very high speed. Extra capacity is provided for resident programs.

The Fairchild model CCD 121 imaging device was replaced with the newer model CCD 121H. A photograph of the ICAS as presently configured is shown in figure 1.

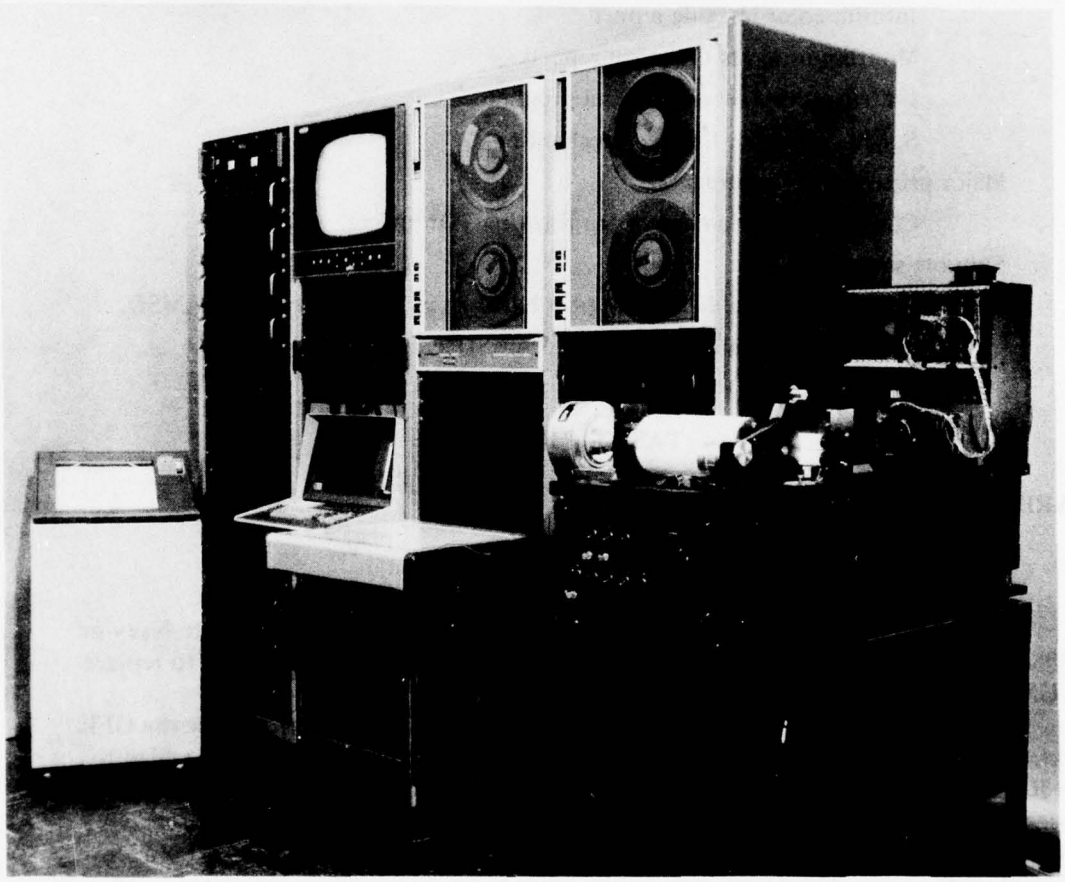

Figure 1. Image Capture and Analysis System.

LARGE DRUM TEST BED

The principal reason for fabricating the large drum test bed (LDTB) was to provide a mounting surface for the copy having the same diameter as the printer, paper-handling equipment/input unit (PPHE/IU) under construction by Pitney Bowes for the USPS. This drum has a circumference of 40.92 inches, chosen to give one pulse output for each 0.005-inch increment of tangential motion from the 8192-pulse-per-revolution Baldwin encoder.

In preparing for some variable resolution tests, a drum having one-third the diameter was turned and fitted with the encoder on the optical bench. With this drum and some electronic modifications, it was possible to scan copy material up to 2400 pels per inch in both directions.

TDI IMAGING

One brief but very encouraging test of time delay integration (TDI) was run using the RCA TC 1155 solid state TV camera using a special version of the SID 51232 area imager. The camera was set up to run continuously at its normal line output rate with the line clocks of the area and storage portions of the arrays tied together. The camera was set at a distance corresponding to 200 picture elements (columns, in this case) per inch in the direction of scan parallel to the drum axis. The proper drum speed was selected to cause the impinging image from the copy to track, as well as possible, the moving potential wells under the surface of the imaging device. The circumferential speed was about 80 inches per second.

A small TV monitor was connected to the video output. Since there was no repetitive vertical sync relationship between drum position and monitor field rate, the resultant pictures were a collection of poorly synchronized flash images. Several of these were photographed with a Polaroid camera. One image was synced closely enough to show excellent resolution in the direction of copy motion around some of the lettering from the IEEE facsimile chart. This simple test brought to light some of the problems to be encountered in operating a TDI device with an independently driven drum. The experience gained from this test was useful in discussions on the driving electronics for the RCA-TDI device and its clocking electronics. A discussion of tests with the TDI imager fabricated specifically for the USPS/NOSC imaging study will be found under Contracts in this summary.

IMAGER DRIVERS

The LDTB was operated with a Fairchild CCD 121 until about midyear, when it was learned that a new and improved imager, the CCD 121H, was available. Procurement was initiated immediately and a design for a new driver board was initiated. This design was fabricated and put into operation upon receipt of the device. There were significant improvements in the balance of odd/even pel output, and the increase in gain afforded by the new on-chip amplifier greatly improved the quality of the images acquired. There still exists, however, an odd/even pel problem of some degree in the acquired data which must be corrected before fully significant data analysis can be completed. This is one of the priority problems to be worked on during the next program year. A discussion of the improved circuits is given in appendix A.

IMAGE ANALYSIS

The Digital Image Analyzer (DIA) was used very little during this year's studies. Instead, software routines were generated which could be used with the Memory Control Unit (MCU). These, of course, could not be run in real time but had several advantages in flexibility not possible with the hardware counterpart. The first advantage was the ability to accept compressibility study run lengths exceeding 64 bits. This single feature provided the ability to determine the exact distribution of extremely long runs, especially in the more-significant bit planes. A second advantage was the ability to broaden the compressibility study to include a new concept of "meander" run length statistics. The combination of these two features led to results containing higher compressibility ratios. Details of these results are included in appendix D. Eventually, if required, these features may be incorporated into the hardware DIA.

PERIPHERAL INTERFACES

During FY77 several interface channels were added to the ICAS:

Input and output between the second Kennedy model 9000 tape deck and the model 9217 format control unit.*

An IEEE-488 interface bus (general-purpose information bus, GPIB) which links together the new model 4051 Tektronix terminal,* the MCU,* the DIA, and the PC. This in turn supplies control signals to the LDTB and the gain and level circuits.

A bus which provides the signal data from the Tektronix terminal to the Versatec printer/plotter* via a Versatec C-TEX2* unit in the printer/plotter.

A high-speed 8-bit parallel bus which supplies bilevel (black/white) image or plot data to the Versatec. This interface was made available by modifying the former Bright tape deck interface which is no longer needed.

SOFTWARE

The USPS/NOSC ICAS is now controlled interactively by a Tektronix 4051 Graphic System via an IEEE-488 GPIB and in conjunction with the ICAS MCU. In this multi-processing organization, the ICAS operator has the capability of executing the various system utility and image processing software in a straightforward procedure-oriented manner. The following paragraphs are brief descriptions of the major software functional groupings available to the ICAS, along with references for greater detail on the individual groupings.

System utility programs are used by the ICAS operator primarily as a means of direct control of storage media including magnetic tape and image memory. Utility programs, however, are also available to other software modules as subroutines designed to simplify major programming tasks. This group of programs includes memory inspection

*These interfaces are operating. The others, except the module for the PC, are designed and installed but not debugged.

and modification routines, tape motion and data transfer routines, and system status routines. (For more detail refer to appendix B of this report.)

Image processing software includes a number of major routine groupings as required by various studies performed on the ICAS. These groupings include resolution testing, adaptive thresholding, meander analysis, and image transformation.

The resolution test software includes LDTB calibration software, to facilitate proper alignment of LDTB components, and image acquisition and formatting routines for use by RCA, Camden (appendix B).

Adaptive thresholding software was used to verify the Fairchild adaptive thresholding algorithm.

Meander analysis is a generic run length analysis using one or more image lines and an arbitrary scan pattern. The statistics generated with this software may then be used by compression ratio software as an aid to determination of optimum run length encoding schemes (appendix D).

Image transformation comprises the largest portion of the image processing software and provides software simulation of proposed hardware prestorage processing algorithms. These algorithms include illumination correction (appendix B), logarithmic compression/expansion,* interpolation, image reformatting, window filtering, and smoothing.

DOCUMENTATION

During the year monthly/technical reports and four specific subject technical reports were written and submitted to AMSD. The reports and the dates of publication are:

Image Capture and Analysis Report	June 1977
Image Resolution Report	July 1977
Advanced Prestorage Processing Report	October 1977
Compressibility Study Report	October 1977

These reports are included in their entirety as appendixes A through D to the annual report. The subject matter, results, and conclusions of these appendixes have been discussed in earlier sections of this report.

The Image Resolution Report was based on the acquisition of data from nine different documents at eight different resolutions up to 600 by 600 pels per inch. Sixty 10½-inch image tapes (approximately 5×10^9 image bits) were generated and provided to RCA Camden for reproduction of the images at the various resolutions. Some of the available reproductions from RCA are included in appendix B.

At the request of USPS, a special 8½-by-8½-inch shortened version of the "standard" WJM typed page document was scanned in two orthogonal directions. The data were stored on tape and will subsequently be used to compare the optimum probabilistic compressibilities for the two scanned directions. The goal is to determine whether there is a potential preferred direction of scan to give the best compressibility.

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*Second Annual Report, Advanced Mail Systems Scanner Technology, NELC TR 2020, Oct 1976

CONTRACTS

The only major procurement contract issued by NELC/NOSC for USPS work was awarded to RCA Princeton in FY76 for development of a tracking/time-delay-integration (TDI) imager. This imager, the RCA TC 1212, has been designed, fabricated, and tested. It contains 96 pels in the TDI direction, divided into a separately controllable section of 32 pels adjacent to the main outputs and a second section of 64 pels adjacent to the alternate outputs. The width of this test imager is 748 pels.

A test driver, providing all bias and clocking voltages to operate the device and amplifiers to recover the image signals, was designed, fabricated, and demonstrated by RCA as part of the contract goals. Although the test driver could not be operated at the maximum design goal speed of 21 megapels per second from each of the four ports, successful operation of the device and the exerciser was demonstrated.

APPENDIX A:
IMAGE CAPTURE
AND
ANALYSIS SYSTEM
THIRD REPORT

Prepared for

US POSTAL SERVICE
June 1977

by

C^2 SYSTEM DEVELOPMENT BRANCH,
TACTICAL COMMAND CONTROL AND NAVIGATION DIVISION
(Code 8242)

NAVAL OCEAN SYSTEMS CENTER
San Diego, CA

CONTENTS

ILLUSTRATIONS

ILLUSTRATIONS (Continued)

TABLES

GLOSSARY

ac	Alternating current
A/D	Analog to digital
address	Peripheral device selection or memory location specification
ALU	Arithmetic/logic unit
ASCII	American Standard Code for Information Interchange
baud	Effective bit rate in bits per second
bit	The smallest piece of digital information – either 0 or 1
bit serial	The bits of a character are transmitted serially
bootstrap	A built-in function which eases system start-up
byte	A logical group of bits (8 is standard)
CCD	Charge-coupled device
CPE	Central processing element
CPU	Central processing unit
D/A	Digital to analog
dc	Direct current
DIA	Digital Image Analyzer
DMA	Direct memory access
DPCM	Differential pulse code modulation
EAROM	Electrically alterable read-only memory
ECL	Emitter-coupled logic
FCU	Format Control Unit
FDS	First difference statistics
FET	Field-effect transistor
Fetch	Microroutine which retrieves MCU instructions from program memory
file	On magnetic tape, a grouping of logical records
filemark	A logical gap between tape files
firmware	System control by use of ROMs and a microprogram sequencer
fpf bit	Front-panel fetch bit; indicates that MCU instruction is from front panel
FSM	Frame-Store Memory
GFE	Government furnished equipment
GPIB	IEEE STD 488-1975 General-Purpose Interface Bus for asynchronous data communications
HCU	Hard-copy unit
HIC	Hardware Illumination Corrector
Hz	Hertz; cycles per second

ICAS	Image Capture and Analysis System
interrecord gap	Physical space between magnetic tape logical records
I/O	Input/output
k	1024
kW	Kilowatts
LDTB	Large Drum Test Bed
LED	Light-emitting diode
LFPM	Linear feet per minute
listener	A device which may receive data on the GPIB
logical record	A logical grouping of data on magnetic tape. In an image, a video line is treated as a logical record
LSI	Large-scale integration
M	Mega-; million
machine language	Operation instructions interpretable by the machine being operated
macroinstruction	A machine language instruction which initiates a sequence of basic machine operations
macrolevel	A level at which an operator may directly communicate with a machine; ie, machine language level
macroprogram	A logical sequence of macroinstructions
MARB	Memory Address Register Bus
MCU	Memory Control Unit
message	On the GPIB, a sequence of data and/or control operations transmitted
MIC	Memory Interface Card
MICC	Memory Interface Control Card
microaddress	Micromemory address
microcode	Bit-by-bit implementation of microinstructions
microcontrol	Control of individual hardware resources by use of a microprogram structure
microinstruction	A basic machine operation instruction containing control for all hardware resources (eg, data paths, registers, ALUs)
microlevel	Hardware direct-control level
micromemory	Memory (usually ROM) which contains micro-instructions
micromemory address	Specification of location within a micromemory
microprogram	A logical sequence of microinstructions
microroutine	A microprogram or part thereof
MIU	Memory Interface Unit
MOS	Metal oxide semiconductor
MSB	Most significant bit

n	Multiplex ratio
NOSC	Naval Ocean Systems Center
ns	Nanosecond
page	An 8½-by-11-inch acquired image or original copy
PBS	Pel brightness statistics
PC	Personality Chassis
pel	Picture element
Pixel	Picture element
PPHE	*Printer and Paper-Handling Equipment*
program	Macro program
PROM	Programmable read-only memory
RALU	Register arithmetic logic unit
RAM	Random-access (read/write) memory
record	Logical record
RLS	Run length statistics
ROM	Read-only memory
SDTB	Small Drum Test Bed
s	Second
SPADE	Storage, Processing, and Display Equipment
t_{mac}	Memory access time
t_{mcy}	Memory cycle time
talker	A device which may transmit asynchronous data on the GPIB
TDI	Time-delay integration
three-wire handshake	The Hewlett-Packard patented method of guaranteeing asynchronous communication capability on the GPIB
TTL	Transistor-transistor logic
USPS	United States Postal Service
UV	Ultraviolet
VTS	Video transmission system
word	A grouping of 1 or more bytes (in the MCU, a word contains 6 bytes, or 48 bits)

EQUIPMENT SUMMARY

Bright Industries	BI2600	Tape drive
Conrac	RQB-17C	Video monitor
Datel	ADC-UH6B	A/D converter
	SHM-UH	Sample/hold module
Fairchild	CCD121	CCD line scanner
	CCD121H	CCD line scanner
	CCD131	CCD line scanner
GTE Sylvania	F18T8H	Fluorescent lamp
Kennedy	9000	Tape drive
	9217	Tape format control unit
Nikon	Micro-Nikkor 55-mm, f3.5	35-mm photographic lens
Phoenix Data	1106-60	A/D converter
	1106-100	A/D converter
RCA	TC1155	Solid State TV Camera
SID	51232	Silicon imaging device
Tektronix	4023	Alphanumeric display terminal
	4051	Graphic System
	4602	Hard-Copy unit
Versatec	1200A	Printer/plotter

REFERENCES

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A2. Naval Electronics Laboratory Center, Second Annual Report Advanced Mail Systems Scanner Technology, NELC TR 2020, October 1976

A3. Institute of Electrical and Electronics Engineers, IEEE Standard Digital Interface for Programmable Instrumentation, IEEE STD 488-1975, ANSI MC1.1-1975, April 4, 1975

A4. Laroff, Gary P, Tektronix GPIB Applications Support, Tektronix, Inc, Boston, 1976

A5. Series 3000 Reference Manual, 98-221A, Intel Corporation, Santa Clara, 1975

A6. Introducing the 3000, Signetics, Sunnyvale

INTRODUCTION

At this time the Image Capture and Analysis System (ICAS) is undergoing some major changes in order to upgrade the image acquisition and processing capability. The major effort is toward increasing the capture speed and image storage capacity so that very high-performance imaging devices can be tested at their maximum capacity. Because of these rather broad changes it was decided to expand the scope of this report beyond the original contractual document requirements which included only the Frame-Store Memory (FSM) and Display portions of the system. Therefore, this report will endeavor to encompass all the modifications now in progress or planned for the test bed.

Because of the broad scope of the subject matter all team members of the program have made contributions to this report. The team members include Frank Martin, Tom Little, Lee Wise, and Clint Mayo. A section on the software by Bob Basinger, who is under contract from SDC, has also been included.

BACKGROUND

Through a series of yearly technical agreements NOSC has been providing assistance to the US Postal Service (USPS) in scanning technology. NOSC is now operating under the third such yearly agreement by providing services under Problem N451, Image Acquisition and Processing. During the first year, the test bed requirements were rather modest. Imaging devices having scan widths of 512 pels or less and an operating speed of less than 10 megapels per second were available. During this period, a Small Drum Test Bed (SDTB) was developed which consisted of an optical bench having a rotating drum 12 inches in circumference and approximately 9 inches wide.* The target area of the drum was illuminated by a 1-kW quartz-iodide, single-filament lamp. During the planning stages of the first test bed, a decision was reached that a special-purpose controller made from high-speed microprocessor chips would offer image acquisition and processing advantages over a slower but more standard minicomputer. The decision appears to have been a valid one. To date the Memory Control Unit (MCU) has proved to be highly adaptable for modification and upgrading to add new interfaces for a number of peripheral devices.

During the second year of the program the SDTB was replaced with a new optical bench and a larger-diameter drum. This drum has a diameter of 13.04 inches and is identical to the scanning station requirements of the Pitney-Bowes equipment under development by the USPS, developed for paper-handling studies. In the new Large Drum Test Bed (LDTB) the incandescent illumination source was replaced with a lamp house enclosing two fluorescent tubes containing phosphors selected for a controlled spectral bandwidth having high intensity in the blue end of the spectrum. This compensates for the poor sensitivity of silicon imagers at the blue end of the visible spectrum. A Baldwin encoder attached to the main drum shaft produces a pulse for every 0.005 inch of motion at the surface of the cylinder. This offers a convenient method of resolution control at 200 picture elements (pels) per inch in the direction of copy motion.

During the second year a GFE (government furnished equipment) Bright Industries tape deck was interfaced to the MCU, providing additional storage capability for image data, permanent records, and programs generated for the capture, display, and processing of images. A GFE display terminal was also interfaced to the MCU allowing convenient operator interface to the system and providing for display of tabular statistical data to be observed and transmitted to a GFE hard-copy unit, a Tektronix Model 4602. Late in the second year of the program a Kennedy Company tape deck was procured which allowed tape-to-tape operations to be performed, thus greatly facilitating the analysis and formatting of image data.

Also during the second year, RCA Princeton began a contract to develop a single very high-speed imaging device which can meet all the USPS scanner requirements at full resolution. It was quickly determined that the USPS/NOSC test bed did not have a capability to accommodate full-scale tests of this type of device, particularly if full-speed images were to be acquired. Further, an assessment of test bed sources throughout industry indicated that no such test facility was available anywhere. For this reason plans were immediately begun to upgrade the test bed to ensure that meaningful, full-scale tests of this type of device (and others like it which may be forthcoming) can be accommodated.

It is intended that this report will serve as a reference document describing the performance capabilities of the upgraded test bed configuration.

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*1 inch ≈ 25.4 mm

SYSTEM CONFIGURATION – DATA FLOW

The significance of the changes being made in upgrading the system can best be described by comparing a block diagram of the existing system with one depicting the system as it is intended to look at the end of the current fiscal year.

FY76 CONFIGURATION

Figure A1 shows the configuration of the ICAS as it existed at the beginning of this contractual year (9 October 1976). At this time, the LDTB shown in the upper left corner of figure A1 was essentially complete including the fluorescent illumination system, the synchronous motors, and the Baldwin encoder. During this period of operation of the ICAS, the principal scanning device used was the Fairchild CCD121. This device provides a scan width of 1728 pels and operates at speeds up to 1 megapel per second, which was adequate for the slow acquisition of images which were acquired, formatted line-by-line in the solid-state memory, and recorded on the Kennedy magnetic tape unit.

Very simple support electronics, derived mostly from Fairchild recommendations, were used to drive the imaging device clock inputs. A simple ac-coupled circuit was provided adjacent to the scanning device to amplify and buffer the output video signal for transmission to the electronics enclosure at the upper rear of the LDTB.

The incoming signal was presented to a Datel SHM-UH sample-and-hold module which stabilized the amplitude of the video signal for an entire clock period.

This stabilized signal was then fed to the Datel ADC-UH6B analog-to-digital (A/D) converter. The A/D converter provided digitization of the analog video signal at a rate of up to 10 megapels per second. The output from the A/D converter was a 6-bit parallel digitized signal which was routed to both the MCU and the Digital Image Analyzer (DIA).

The MCU accepted the 6-bit pel data and, through the use of an input-packing circuit, formatted eight such 6-bit samples into a single 48-bit digital word which was then available for transmission and storage into the semiconductor Frame-Store Memory (FSM). During acquisition of an image, the MCU continued to accept digital data in this manner from the A/D converter until a line of data had been acquired. The process then continued as additional lines of data were made available from the CCD scanning device, until the entire image capacity of the FSM was filled or until an entire page of data had been captured. The MCU was capable of transmitting 48-bit data words to the FSM and was also capable of providing addresses for the recall of data words from the memory in accordance with control instructions within the MCU itself.

The capacity of the FSM was exceeded when a full page of image data was recorded. The only way to provide storage for the entire image page was to record the information digitally onto magnetic tape. Data from the MCU were recalled from the FSM on a line-by-line basis and broken into 8-bit bytes which were then presented to the Kennedy Format Control Unit (FCU) and passed on to the Kennedy tape deck for permanent recording. Other data such as programs and data files could be written on the magnetic tape under the control of the Tektronix 4023 terminal which was provided as GFE during this period of test bed operation. Data could also be retrieved from the Kennedy tape deck and transferred via the MCU to the FSM. By use of the MCU it was also possible to retrieve a subset of a page of image data from the FSM and reformat it into 6-bit pels, which were transferred for display to the Conrac RQB-17 Monitor which was furnished as GFE during this phase of the test operation.

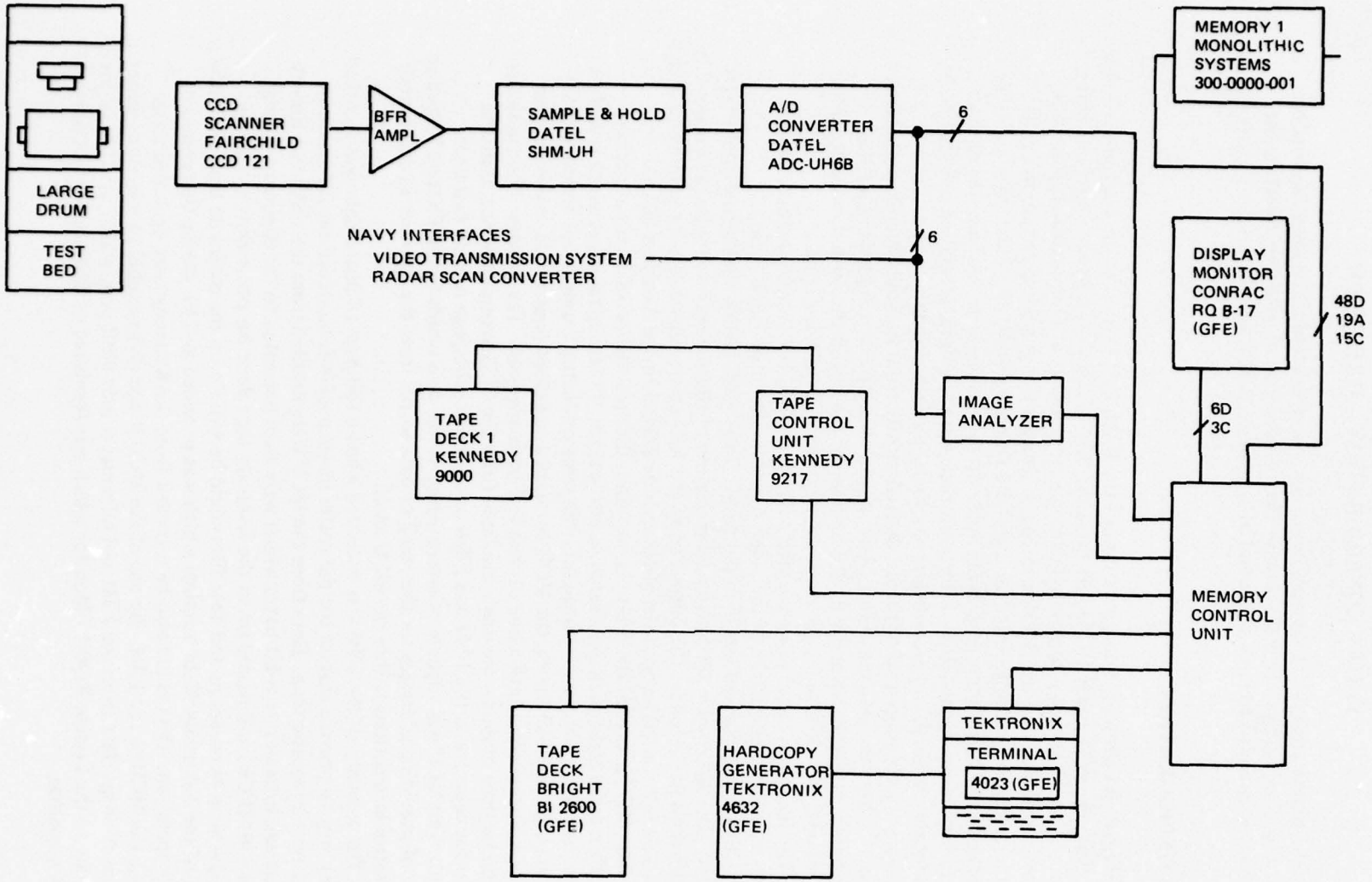


Figure A1. Image Capture and Analysis System – FY76 configuration

The digital 6-bit output from the A/D converter was also presented to the DIA. The DIA was capable of accepting these 6-bit pels at a rate of 21 megapels per second. The DIA was capable of operating in 30 different modes. These modes included pel brightness statistics (PBS), first difference statistics (FDS), and run length statistics (RLS) modes, each in either binary or Gray code. The DIA had the capacity to store the statistical data in any of these modes (8½ by 11 inches) at 200 by 200 pels to the square inch. Data were stored in 64 memory locations, each location with a capacity of 24 bits capable of accumulating a total of approximately 16 000 000 statistical increments. At the end of a page of data analysis, the contents of the 64 memory locations were transmitted to the MCU, where they were in turn converted from binary to decimal representation and transmitted to the Tektronix Model 4023 terminal for visual presentation. The terminal had a direct connection to a Tektronix 4602 Hard-Copy Unit (HCU) which allowed displayed data to be printed for permanent records. The HCU was also made available as GFE during this phase of the ICAS operation.

Although simple, this configuration of the system was capable of performing a number of useful tests supporting the characterization and limitation analysis of CCD scanning devices. A great deal of meaningful data was acquired by the use of this configuration. Reference A1 presents some of the theory on which data acquisition investigations have been based. Data on prestorage processing, compression, image enhancement, and image storage and retrieval are presented in NELC TR 2020 (ref A2).

UPGRADED CONFIGURATION

On 15 March 1976 NOSC awarded a contract to RCA Princeton for the design, fabrication, and delivery of a very high-speed imaging device which could accommodate most of the high-speed image acquisition goals of the USPS. Delivery of the first sample of this imager was made 15 June 1977. The configuration of this imager is quite unlike that of any previous scanning device. It provides four parallel output channels each having a video rate of 21 megapels per second. The device operates in the time-delay integration (TDI) mode. Because of the simultaneous high-speed output into four separate channels there is a requirement for a corresponding four-channel acquisition path in the ICAS. In order to evaluate and characterize the device at its design goal speed, it is necessary that all four channels of the data path be compatible with the 21-megapel-per-second video data.

Another reason for upgrading the test bed was to remove the GFE which had been borrowed from Navy programs. The Navy programs were beginning to utilize these equipments to an extent which would eventually cause scheduling conflicts in the performance of tests.

Figure A2 is a block diagram of the upgraded system configuration. There are three significant features to this block diagram. The first is that a four-channel capability is required beginning at the imaging device itself and continuing until the data reach the "personality" modules. The second feature is the greatly expanded memory requirement for full-page images to be captured at the required speed. The third feature is the significant fact that none of the equipment required to support the tests is GFE.

A1 Naval Electronics Laboratory Center, First Annual Report Advanced Mail Systems Scanner Technology, NELC TR 1965, October 22, 1975

A2 Naval Electronics Laboratory Center, Second Annual Report Advanced Mail Systems Scanner Technology, NELC TR 2020 October 1976

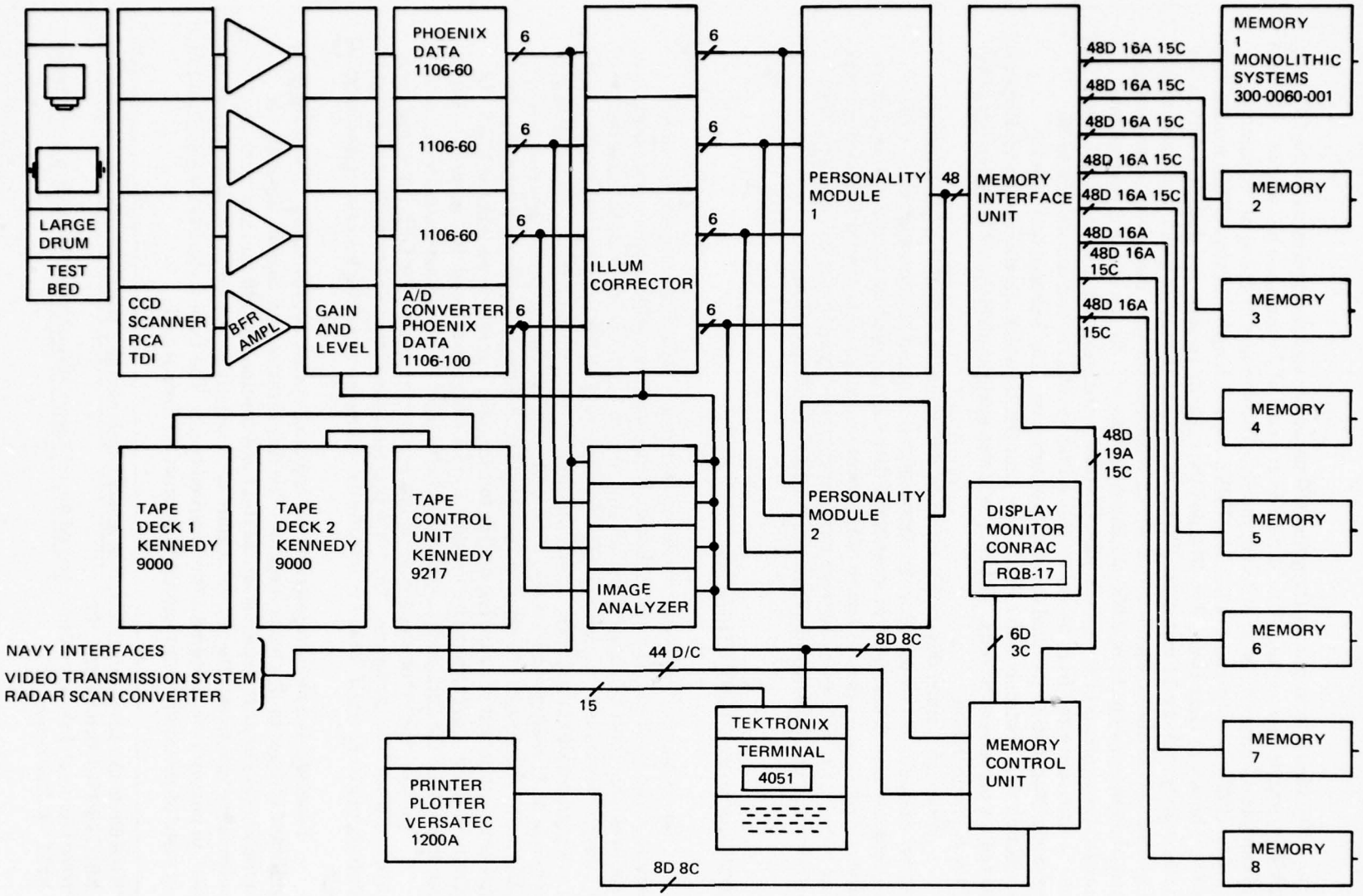


Figure A2. Image Capture and Analysis System — upgraded configuration.

No major modifications are required of or upon the LDTB. The same lens, drum, and illumination source are expected to be adequate for operation of the RCA TDI imager.

The clock driver board which formerly supported the Fairchild CCD121 imager will be replaced by the four-channel RCA device driver which will be shipped from Princeton. The four channels of output video data will be buffered so that they can be sent to the Storage, Processing, Analysis and Display Equipment (SPADE). The sample-and-hold and A/D converter modules now residing in the simple electronics card bin on top of the LDTB will be bypassed and the functions of multichannel digitization will be accomplished in the SPADE.

The functions of all modules of the test bed are outlined here and are completely covered in the body of this report. This simplified description will provide the reader an overview of the detailed description which follows. It also may be helpful in following the continuity of data flow through the system.

After data are transmitted in four analog video streams from the LDTB to the SPADE, the signals are fed to the gain and level circuits. The gain and level circuits are included in the same enclosure as the Phoenix Data A/D converter modules. It is the purpose of the gain and level circuits to provide offset and amplification of the analog signals. Adjustments will be made to the illumination level in the LDTB and the gain of the buffer amplifiers so that the full dynamic response range (from white to black) of the CCD imager will be reached when $BaSO_4$ (barium sulfate) white standard and black felt targets, respectively, are used for calibration. Normal dynamic response from copy substrates having less reflectance than the white standard and imprinted with ink having more reflectance than the black standard will not utilize the full dynamic range of the ICAS. By increasing the gain of the video signal and adjusting the bias (the dc level), it is possible to adjust the video signal so that it utilizes almost all the dynamic range of the A/D converter and the remainder of the system. Control signals indicating the desired gain and level settings will be generated within the MCU. These signals will be sent to all four gain and level modules, which will be simultaneously adjusted to the same values of gain and level. The outputs from the gain and level circuits will be buffered to operate between −2 and +2 volts and will have a low output impedance.

The data will then be converted to 6-bit digital signals by the set of four Phoenix Data A/D converters. The input voltage will range between −2 and +2 volts. There will be three model 1106-60 A/D converters, each with a capability of operating at rates up to 60 million conversions per second. There will also be one model 1106-100 A/D converter which has an operating capability up to 100 million conversions per second. The choice of A/D converters stems from the fact that the maximum speed required from a four-channel scanning device is 21 megapels per second. This speed can be accommodated by the model 1106-60. If a two-channel device were to be developed and 42 megapels per second were required, two of the 1106-60 devices would be capable of providing the 6-bit conversion. In the event that a flying-spot scanner or an extremely high-speed imager having the single-channel capability of 84 megapels per second were to be developed in the future, the single 1106-100 would be capable of handling the 84-megapel-per-second data rate. In other words, the choice of A/D converters selected allows for future growth by permitting the system to accept new devices as they become available.

Because of the cable lengths required between the A/D converter and the modules to which the outputs are connected, all signals leaving the A/D converter enclosure will be balanced-differential emitter-coupled logic (ECL) data and control paths. The outputs from the A/D converter enclosure will be presented to the DIA.

The DIA already exists as described in the FY76 test bed report. Upon demand, analysis data will be transmitted from the DIA to the MCU via the IEEE 488 (GPIB) interface. (The FY76 configuration required a separate interface.) At present the DIA accepts a single channel of pel data at rates up to 21 megapels per second. If a requirement exists for full-page analysis, including all four channels at 21 megapels per second each, three more modules almost identical to the existing one would be required. At the present time the other three modules are not under consideration for two reasons. It may be possible to obtain sufficient analysis data on a less than fully populated sample of page data in order to make a determination as to the type of image being acquired. In other words, it will probably be permissible to acquire every fourth pel in a page of data and obtain proportionately the same statistical distribution of events as if the full 22.44 megapels per page were analyzed. Also, this concept can be verified by storing the full page of data and analyzing the entire 22.44-megapel page at a slower rate. The other three modules of the DIA would then be fabricated only if absolutely necessary.

Another 24-pair set of balanced-differential ECL signals is fed from the A/D converter enclosure to either the Hardware Illumination Corrector (HIC) or, bypassing this function, directly to the Personality Chassis (PC). Although the HIC has not been fabricated, the plans for a version accepting data at a 21-megapel-per-second rate have been detailed. Calibration data for the HIC are obtained by scanning a section of "white standard" material across the entire width of the copy and using the resulting response profile as calibration input. By using the calibration curve on a line-by-line basis, pel values can be provided at the output which are normalized against nonuniformity of response resulting from illumination source optical shading and imaging device response nonuniformity. A decision to provide three other modules of the illumination corrector which would allow operation at the full rate of 84 megapels per second will be postponed until the performance of the first module has been tested.

The 24 pairs of balanced-differential ECL signals emerging either from the A/D converter enclosure or a fully populated HIC are fed to the PC. It is the function of this equipment to accept digital pel data from a variety of imaging devices at rates of up to 84 megapels per second. This equipment formats the data into sequences of 48-bit digital words which, when routed through the Memory Interface Unit (MIU), can be selectively stored in the eight semiconductor memory modules. Because of the wide variety of imaging device outputs it is expected that a number of different personality modules may be required in order to satisfy the rather unique, but very high-speed, data rates required from each imager or set of imagers under test. An example of a very complicated interface for the RCA TDI imager is described in the body of this report. If room permits, more than one personality module will reside in the PC at one time so that imaging devices can be exchanged on the test bed without the need for reloading an entire set of circuit boards for each type.

As mentioned, the output of the PC consists of 48-bit digital words representing the brightness levels of eight adjacent picture elements. These are fed to the Memory Interface Unit (MIU), where they are demultiplexed to one of the eight solid-state FSM modules. The MIU acts as a distributor, or "dealer" for the 48-bit words. In most cases 64 pels are demultiplexed into 48-bit words which are sent simultaneously, one to each of the eight FSM modules.

The FSM modules accept the data as distributed from the MIU and store the data in buffer registers until a write command is issued by the MIU. The write command is given to all eight modules simultaneously and the words are then stored into locations within the FSM.

Address locations for the data storage are generated and transmitted to the memory modules by the MIU. The addresses for storage within the memory will not necessarily be sequential because the data accumulated by the test bed may come from portions of the imaging device which are viewing different portions of the copy on the LDTB. In almost all cases an attempt will be made to store the data in the FSM in such a fashion that sequential retrieval addresses can be given for the withdrawal and presentation of a full page of copy.

At the present time there is no plan to attempt to retrieve the information from the memory modules at the same high-speed rate at which it was recorded, but provisions are being made so that at a later time, if it is desirable to exercise or stress a communication system with data at-speed, this feature can be added to the test bed.

The MCU is the master control center for the entire test bed. This unit can operate on 48-bit words and is connected directly to the MIU so that two-way data can be transmitted between the MIU and the MCU. Software algorithms can be executed on image data to prove the feasibility of such enhancement and compression techniques as may be required. The MCU also provides a high-speed data output port to the Versatec model 1200A Printer/Plotter and an I/O port compatible with the IEEE GPIB which controls the operation of the HIC, DIA, and gain and level circuits. It also provides a compatible I/O channel to the Kennedy model 9217 FCU which in turn controls two model 9000 tape decks. By use of the MCU and the MIU, data can be transmitted between tape storage and semiconductor memory in either direction.

A Tektronix model 4051 terminal is connected to both the GPIB and the Versatec 1200A. It is possible to perform most of the man-machine interaction with the imaging test bed via this terminal. The connection to the printer/plotter provides a method of producing hard-copy records of data presented on the terminal display.

There exists an input to the system which allows Navy data, such as from a video transmission system (VTS) or from a radar scan converter, to be entered into the test bed. This provides a method whereby Navy data can be analyzed and processed by the ICAS.

A Conrac RQB-17C video monitor is also provided in the test bed. This display allows high-quality presentation of portions of the image data. Typically the area of display is limited to approximately 440 by 440 pels per second at a flicker-free rate. The 64 grey-scale brightness levels afforded by 6-bit digital data can be accommodated by the monitor system.

This completes a general description of the data flow through the system. Figure A3 depicts the planned physical layout of the entire ICAS. The more detailed description which follows will amplify the operation descriptions of each of the modular functions which are incorporated in the test bed.

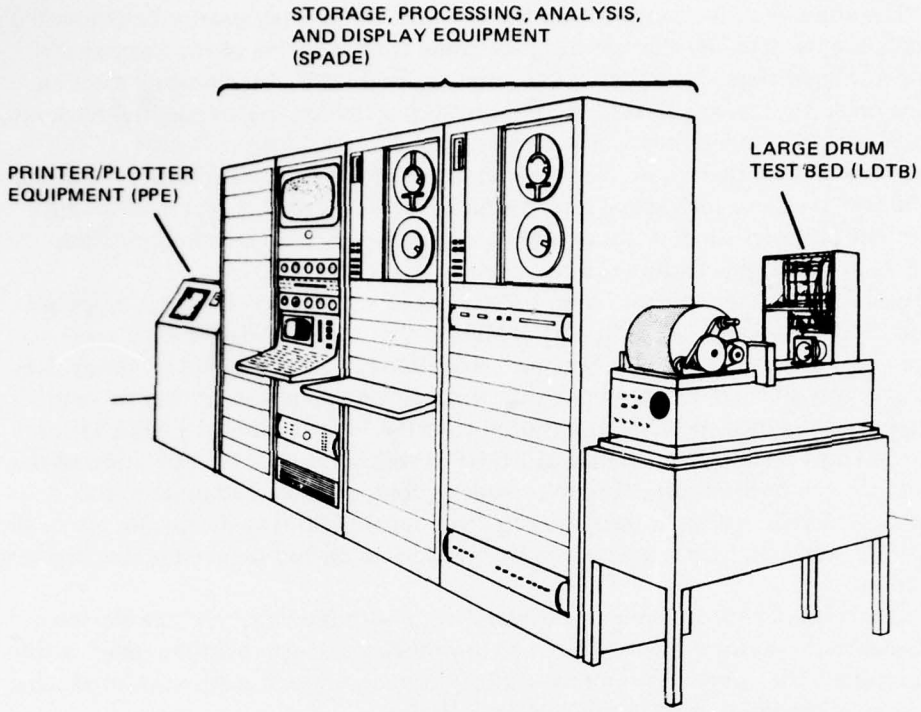


Figure A3. Image capture and analysis system (ICAS).

SYSTEM DESCRIPTION

This section describes each major function of the ICAS. Data for those portions of the system which remained unchanged from the FY76 system have been taken from the FY76 annual report. New functions which have been designed but are not yet operational will be described as they are expected to perform after being integrated into the system.

It is the goal of the report to provide a comprehensive description of the system and its capabilities. It is not intended that this document be used as a maintenance, software design, or operator's manual.

LARGE DRUM TEST BED (LDTB)

Figure A4 shows the LDTB as configured in FY76. During FY76 the imager used was a Fairchild CCD121 1728-element linear array. The circuit card enclosure presently contains digital clock and control logic, sample-and-hold module, A/D converter, and line drivers for both the DIA and the MCU. A detailed description of the FY76 LDTB can be found in reference A2, appendix C.

In the upgraded configuration, the sample-and-hold module and the A/D converter will be replaced by four high-speed A/D converters, each with an integral sample-and-hold amplifier.

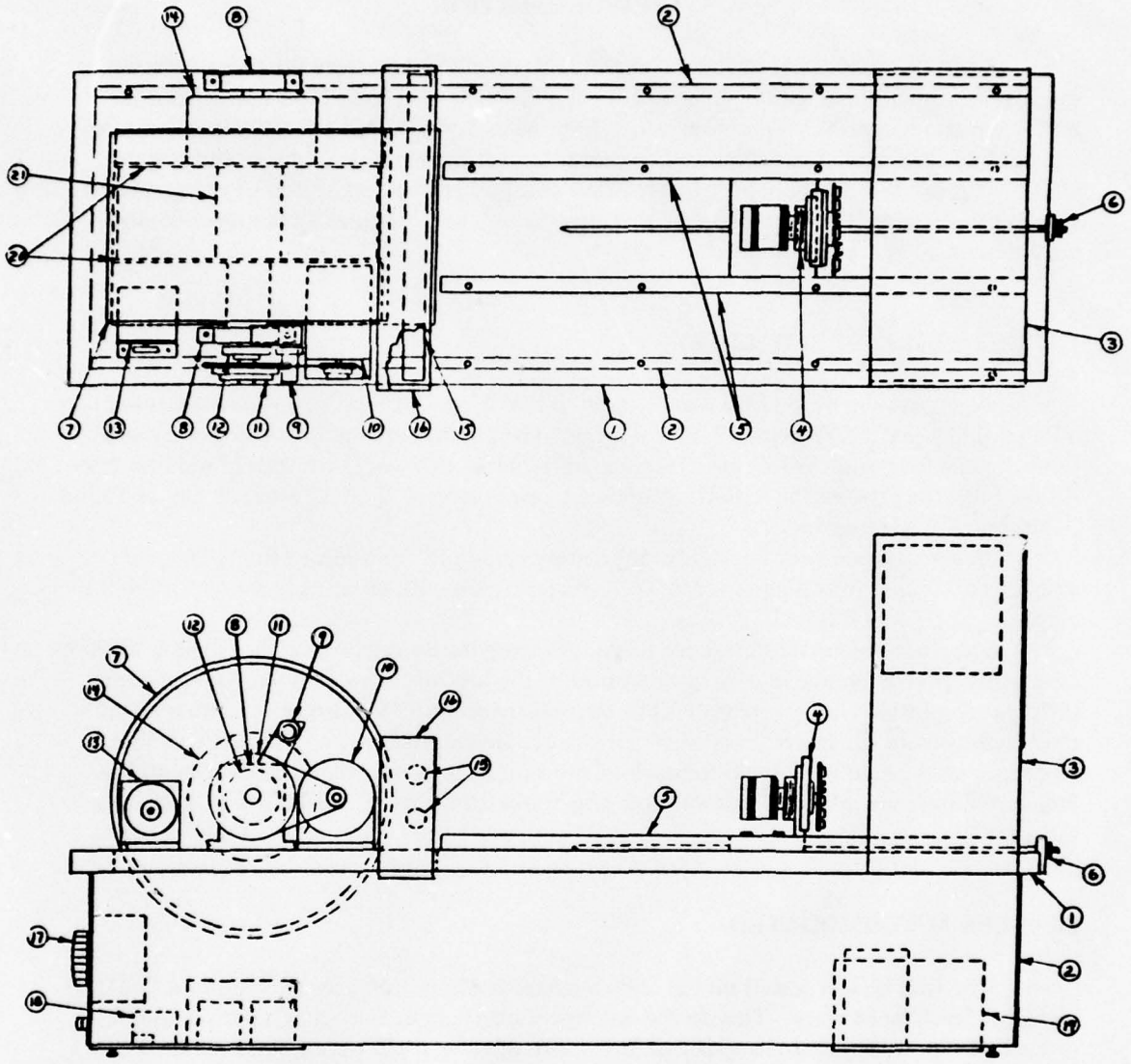
The 40.96-inch-circumference drum was temporarily replaced with a smaller drum of 13.65-inch circumference in order to accomplish the task of scanning documents at eight different resolutions ranging from 120 to 600 pels per inch. This allowed the quadrature clock pulses from the incremental shaft encoder to be counted down in such a way that line-rate pulses could be derived for each of the various resolutions required. The 40.96-inch-circumference drum affords a flatter target area and is the one used for TDI tests on the LDTB.

IMAGERS ACCOMMODATED

The first imager tested on the early system configuration was the Fairchild CCD110 imager, 256-element array. This device was operated at about 9 megapels per second in order to demonstrate image acquisition capability at close to 20 pages per second. A necessary assumption was that eight of these imagers could be optically abutted in order to scan the entire 8½-inch dimension of a page at a resolution of 200 lines per inch.

After a magnetic tape unit was acquired and added to the system, the capability was expanded for the capture and storage of full-page images on magnetic tape. To acquire full images, a CCD121 imager (a 1728-element linear array) was installed. Because of speed limitations of the magnetic tape unit, image acquisition is accomplished at very slow speeds – on the order of 115 kilopels per second.

Several problems were encountered with the CCD121. The first was a difference in output levels of the analog charge transport registers. Another problem was a dc offset when the compensation amplifier portion of the chip was illuminated. This required that the output from the imager be ac-coupled to the video preamplifier. A third problem involved the low operating speed of the device. In order to maintain linearity at very low operating speeds, the devices must be specially selected.



Drum Support Bearing Blocks	8	Lamp Housing	16		
41-Inch-Circumference Drum	7	Fluorescent Lamps	15		
Scanner Fine Focus Adjust	6	Shaft Encoder	14		
Scanner Adjust Guides	5	½ RPM Motor Assembly	13	Drum Shaft	21
Scanner Assembly	4	1-Step Aux Pulley	12	Drum Support Plates	20
Circuit Board Enclosure	3	3-Step Pulley	11	Card Enclosure Power Supplies	19
Bench Support Rails	2	900-RPM Motor Assembly	10	Lamp Power Supply	18
Bench Top	1	Jack Shaft Assembly	9	Power Control Panel	17

Figure A4. 40-inch-circumference drum test bed.

These problems were largely alleviated with a later design of the CCD121H imager. The newer design contains added metalization to prevent the "odd-even" problem in the transport registers and the "peripheral vision" around the compensation amplifier. In addition, this new design contains an internal preamplifier which boosts the video output level to about 700 mV from the original 100. The selected CCD121H imager provided far superior performance than the first CCD121.

Another imager that has been tested very briefly on the LDTB is the RCA TC1155 solid-state television camera which uses the SID 51232 area-imaging device. In normal operation the camera is a standard 525-line, closed-circuit TV camera with a resolution of 320 pels per line; however, it has been modified to operate in the time-delay integration (TDI) mode. A detailed description of TDI operation can be found in reference A2, page C-47.

Future imagers to be tested on the LDTB are the newly fabricated prototype tracking-imager chips from RCA, a CCD131 imager organized as a 1024-by-1 linear array, and the Scanning Subsystem for the USPS printer and paper-handling equipment (PPHE) input unit designed by Fairchild which contains two optically abutted CCD131 imagers.

BUFFER AMPLIFIERS

For testing the CCD110 imagers, the buffer amplifier in figure A5 was used with two modifications. The capacitive coupling on the output of the 733 video amplifier and the dc-clamp circuits were not used. In that configuration the CCD110 imager was tested at pel rates of up to about 9 megapels per second. The overall bandwidth of the buffer amplifier is about 40 MHz.

When the CCD121 was installed in the test bed and run at much slower rates, the problem of low-frequency drift became apparent. A technique of dc coupling was attempted. There was, however, a dc level shift which was attributed to stray illumination falling on the chip in the vicinity of the compensation amplifier. As an alternative, the dc clamp circuit shown was used. This circuit has a speed limitation of about 1 MHz due to the level-shifter circuits. Since all work thus far utilized the magnetic tape unit for image storage, the imager has been operated at speeds well under 1 MHz. A discrete level shifter may be necessary when the full-page frame-store memory is implemented, in order to allow higher-speed image acquisition.

The new-design CCD121H contains an on-chip preamplifier which provides a peak video output of 600–700 mV instead of 100–200 as on the CCD121. With this increased output level the 733 video amplifier was no longer needed. Also, with the older configuration of the ICAS, full-size images had to be stored on magnetic tape as they were acquired. The time required to write an image line (1728 pels) on tape is about 37 ms. Therefore, image acquisition was a necessarily slow process with the imager operating at about 114 kHz. With this slow speed the 40-MHz differential amplifier could be replaced with a simpler high-speed operational amplifier allowing a wider range of control over the gain and level of the video output. A schematic of this amplifier is shown in figure A6.

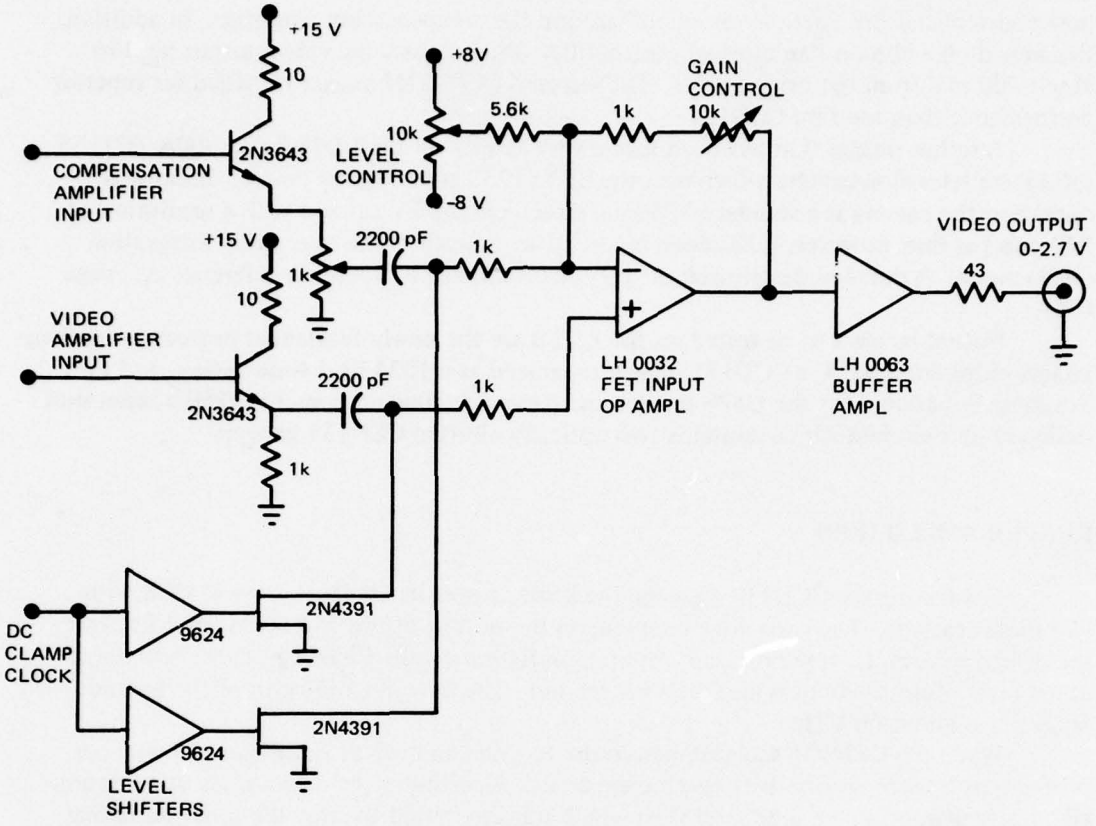


Figure A5. Buffer amplifier for CCD121H.

As the ICAS is upgraded with the addition of the full frame-store memory, the rates at which images may be scanned will be limited by the imaging devices and associated circuitry. At this time the output from the CCD121H will be amplified and level-shifted by the digitally controlled gain and level circuitry now in fabrication. The buffer amplifier associated with the imager will then be an LH0033 unity-gain buffer amplifier which will drive a 50-ohm coaxial cable. The LH0033 has a bandwidth in excess of 50 MHz.

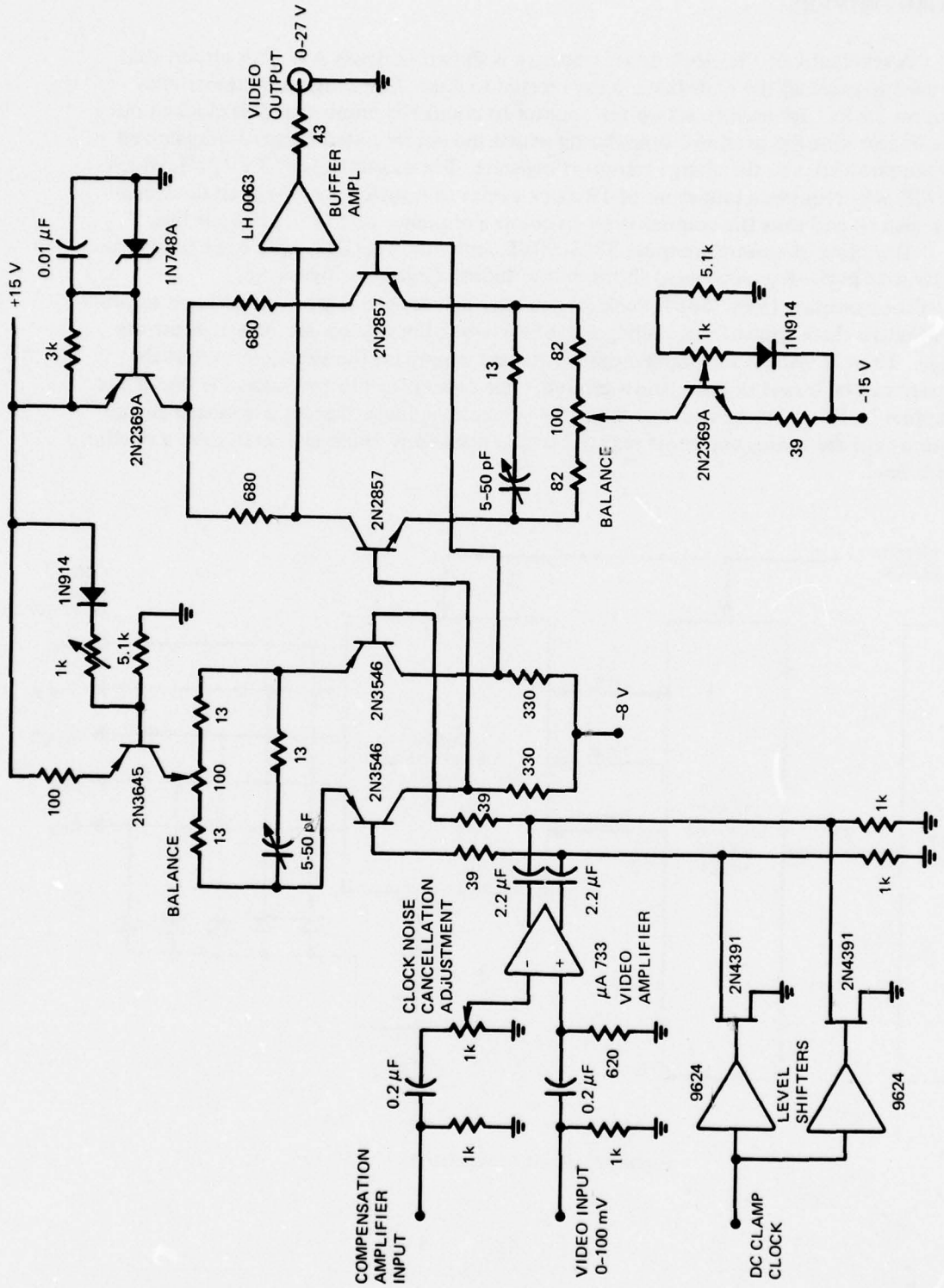


Figure A6. Buffer amplifier CCD110 and CCD121.

IMAGER DRIVERS

A schematic of the clock driver circuitry is shown in figure A7. This circuit has been used to drive all the CCD linear arrays tested to date. The programming switches shown on the left are used to set up the counter to count the number of pels clocked out of the imager plus the overhead time during which the accumulated charge is transferred from the photosites to the charge transport registers. For example, the CCD121H, which has 1728 pels, requires a minimum of 19 clock cycles to transfer the charge to the transport registers, and thus the counter is set to count a sequence of 1747 cycles per line.

Decoding of counter outputs 7755, 7765, and 7767 (octal) is used to generate the transfer gate pulses ϕ_{XA} and ϕ_{XB} shown in the timing diagram in figure A8.

Clock outputs from 75451 clock drivers have a diode clamping network used to prevent negative clock spikes from pulling any of the clock lines below the imager substrate voltage. There is also an adjustable negative voltage supply on the substrate so that the substrate can be biased slightly below ground. The reason for this precaution is that if the clock lines go below (more negative than) the substrate voltage, there is a resulting charge injection into the analog transport registers which masks any video information in a portion of each line.

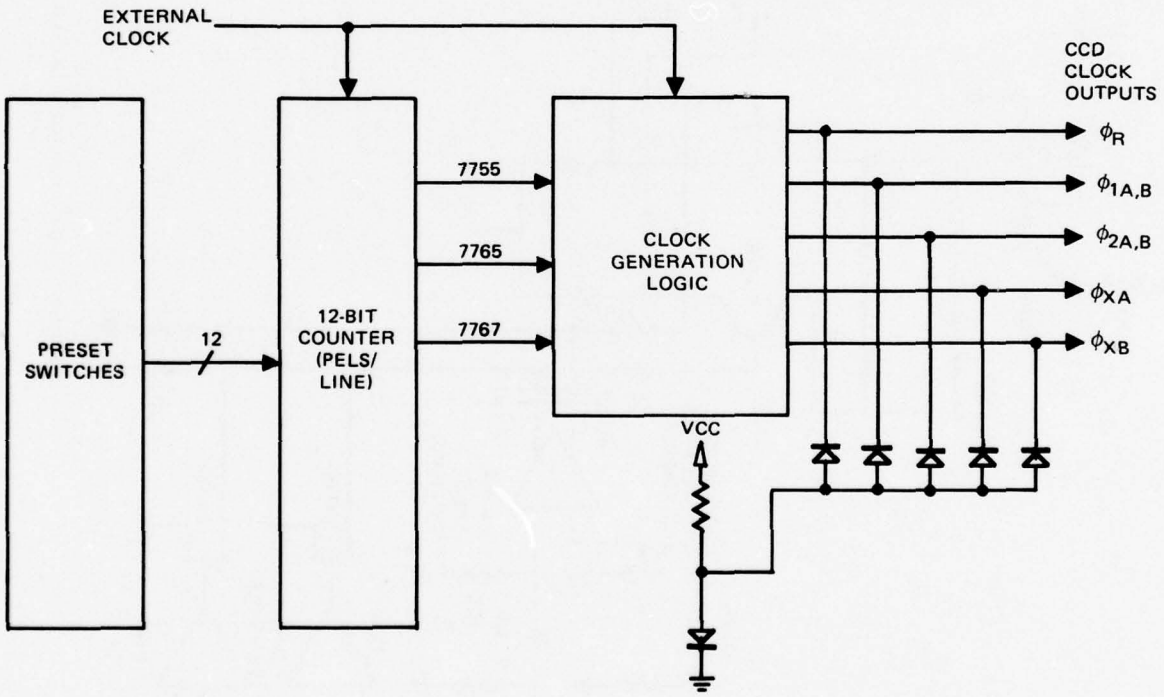


Figure A7. Clock driver circuit.

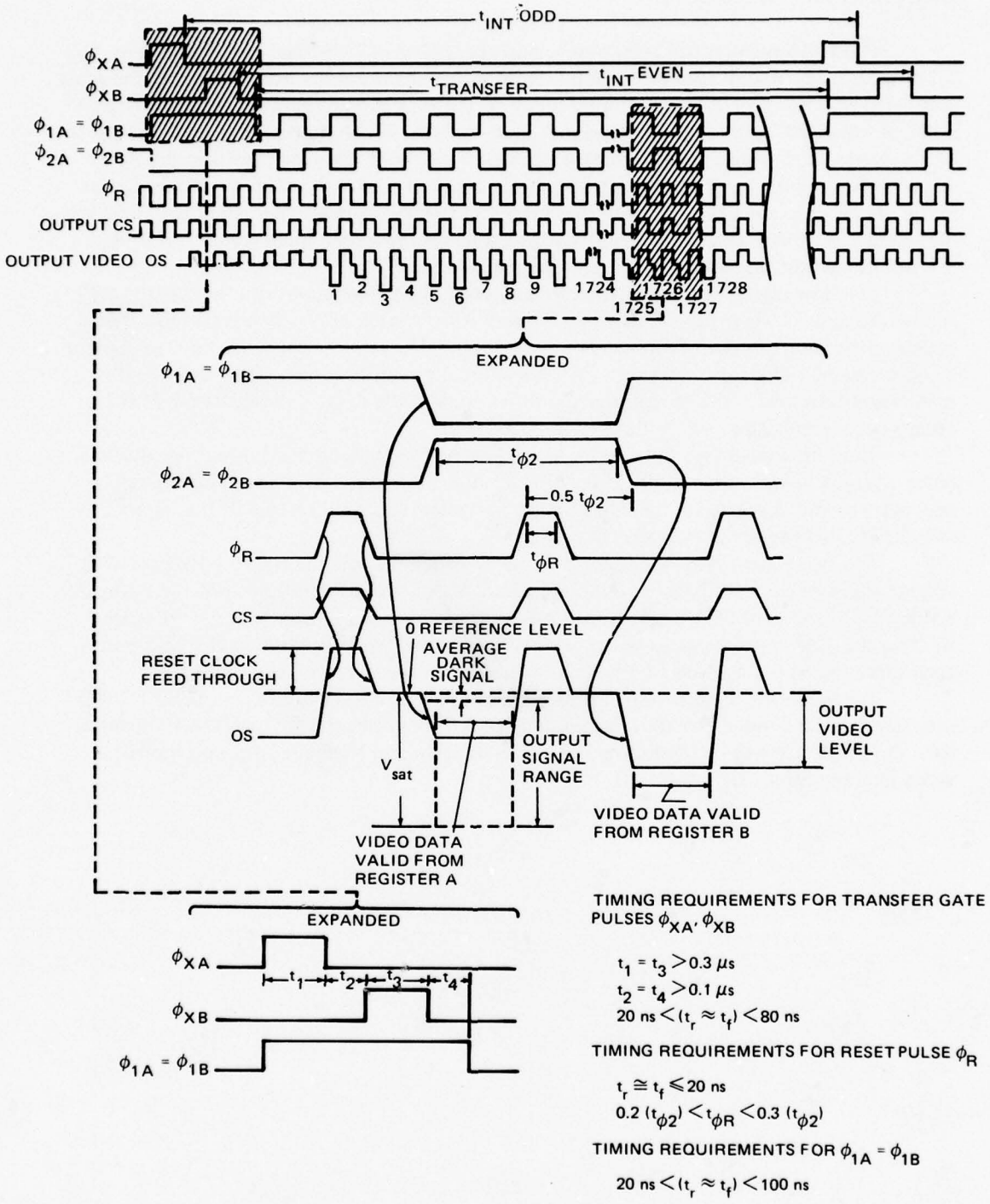


Figure A8. Transfer gate timing diagram.

GAIN AND LEVEL CIRCUITS

The ICAS scanner can be set up to perform either of two functions required by the proposed advanced mail scanner system (see ref A2). These are the prescanner and the main scanner functions. For the prescanning function the gain and level are set up according to a "black standard" and a "white standard" range outside which no real video is expected to be received. Thus, video image data from mail copy will fall somewhere within the A/D converter's dynamic range. After a prescan it is a function of the system controller to use image statistics to calculate values of level and gain for the main scanner function. This will allow the same image data subsequently scanned by the proposed main scanner to utilize the full dynamic range of the A/D converter subsystem.

To allow digital control of the gain and level of a video amplifier, the circuitry of figures A9 and A10 is used. At the top of figure A9 is a latch into which is stored a 3-bit code representing one of eight possible level settings. The latch outputs are used to control a resistive-ladder current-switch on a 741 operational amplifier input. The two potentiometers associated with the operational amplifier control the range and sensitivity of the binary code, resulting in a very flexible level control.

The gain adjustment is made by a series of FET switches arranged in a signal attenuator circuit shown in the middle of figure A9. A 2-bit digital code is stored in a latch (not shown) and decoded by the 7442 decoder to select and turn on one of the four FET switches to provide the overall gain desired.

The two-stage video amplifiers, a detail of which is shown in figure A10, provide a voltage gain of about 14 dB from dc to 40 MHz. With the configuration shown in figure A9, a video input signal of 0–700 mV is amplified and level-shifted to obtain a ±2-volt output to drive the A/D converter subsystem. For this operation the minimum gain is selected, corresponding to the bottom FET's being turned on in the gain and level amplifier.

To obtain the digital control signals for the gain and level circuits, an IEEE (GPIB) interface will be designed to allow communication from either the MCU or the 4051 terminal. This interface will be used to control both the gain and level circuitry and the HIC when implemented.

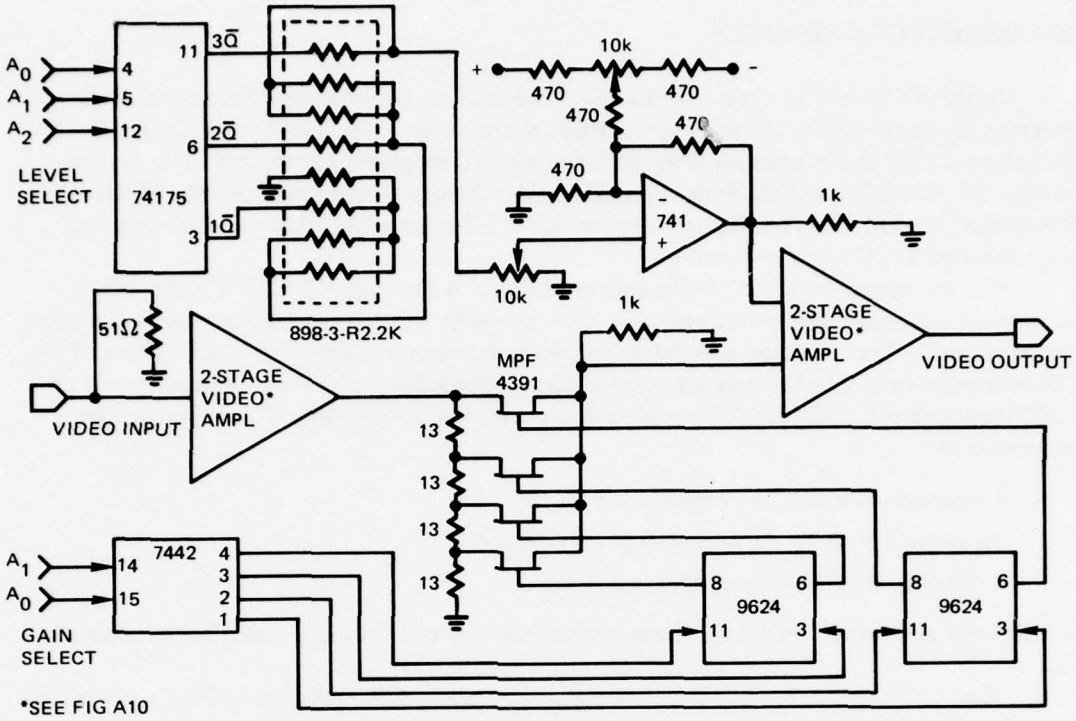


Figure A9. Gain and level amplifier with digital control.

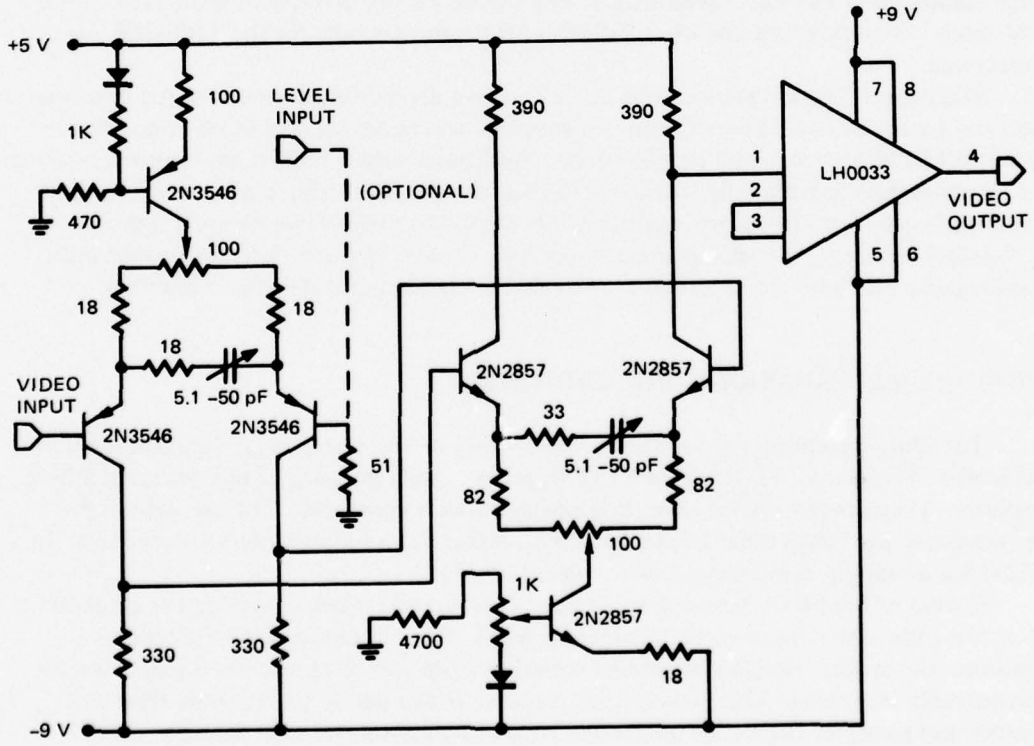


Figure A10. Two-stage video amplifier.

A/D CONVERTER SUBSYSTEM

In the FY76 configuration of the ICAS the sample-and-hold module and the A/D converter are Datel's SHM-UH and ADC-UH6B, respectively. These units provide single-channel capability at a maximum throughput rate of 10 megapels per second. For system operation this was the maximum design goal of the memory control unit and the CCD110 256-element imager. This configuration provided a 1/8-page acquisition capability in real-time operation at 20 pages per second.

For the upgraded ICAS configuration, the goal is the acquisition of a full 8½-by-11-inch page at a 20-page-per-second rate. To accommodate this rate with a four-channel imager, a four-channel A/D conversion subsystem has been incorporated into the ICAS. Three of the A/D converters operate at speeds up to 60 megapels per second and the fourth at speeds up to 100 megapels per second. This subsystem can thus handle a variety of imager configurations such as:

4 channels at up to 21 megapels per second each

2 channels at up to 42 megapels per second each

1 channel at up to 84 megapels per second

With suitable analog multiplexing, imagers with more output channels could be accommodated.

These A/D converters are Phoenix Data Inc models ADC 1106-60 and ADC 1106-100. Each of these converters employs a parallel conversion technique utilizing a series of 63 voltage comparators and high-speed ECL to encode the 63 comparator outputs into a 6-bit digital value. Encoding time for the 1106-60 is 16.6 nanoseconds; for the 1106-100, 10 nanoseconds.

The four A/D converters will be housed in two 8¾-inch rack-mount units, two converters per enclosure, with necessary power supplies, forced air cooling (each converter requires 500 LFPM air flow), and signal buffers. Additional signal buffers are required because the A/D converters provide only single-ended ECL signals. The cabling path is too long for single-ended operation; therefore, buffers will be added to drive all signals differentially over twisted-pair lines. It is also planned to include in each of these two rack-mount units the analog gain and level circuits used to provide the analog inputs for the converters.

HARDWARE ILLUMINATION CORRECTOR (HIC)

The illumination source for the LDTB consists of two special high-brightness fluorescent lamps. These are GTE Sylvania F18T8H lamps with a mixture of red, green, and blue phosphors. They are nominally 33-watt lamps in 15-watt envelopes. For use with high-speed scanners, the lamps must be operated with either dc or high-frequency ac voltage. In the LDTB a dc supply mounted below the drum is used.

Curves of brightness across fluorescent tubes show a brightness reduction of about 14% at the ends with respect to the center (fig A11). When mounted and enclosed in a lamphouse, the actual reflected brightness variation from end to end across a uniform page is considerably increased. This nonuniform response is due partly to the finite length of the tubes and partly to the design and reflectance of components in the interior of the lamphouse.

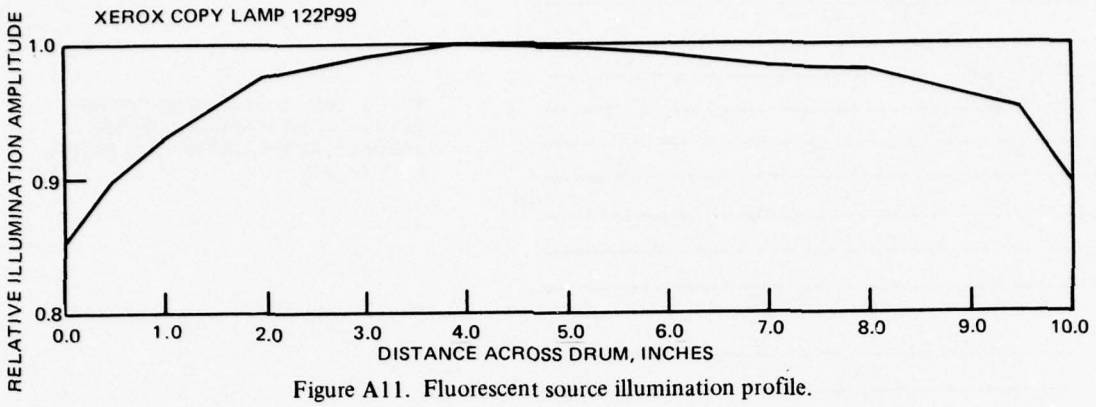


Figure A11. Fluorescent source illumination profile.

There are additional sources of nonuniformity of optical response in the system. These sources are related to charge transfer efficiency and to variation in response of the individual photosites of the imaging device.

Another contributor to nonuniform response of imagers is related to the quality and proximity of the lens assembly. The LDTB employs the Micro Auto Nikkor P55 f3.5 lens. This photographic lens is one of the sharpest lenses available for 35-mm photography, and has a very high center-to-edge resolving power. It also has an extreme flatness of field and high image contrast.

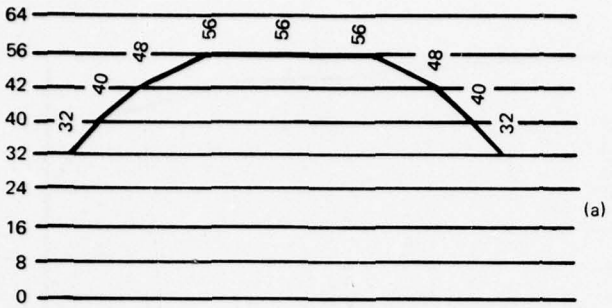
The initial studies of illumination correction were made by using the MCU and the FSM. These attempts were shown to be slow and laborious because it was necessary to use the magnetic tape deck for retrieval and storage of uncompensated and compensated images. Accordingly, a hardware illumination corrector (HIC) capable of real-time operation at 21 megapels per second has been designed (but not fabricated) for future compensation studies.

In both the aforementioned approaches, ie, the software and hardware implementations, the simplest strategy devised thus far can be seen in figure A12. This method requires that a calibration scan be taken of a uniform target of the whitest material available. Eastman white reflectance paint, which is barium sulfate mixed with a binder material, was selected for our application. This white reflectance paint was sprayed onto a rigid bar which in turn can be mounted on the test drum. The acquired calibration curve will have an appearance similar to that shown in figure A12(a). The process is continued as further described in the figure.

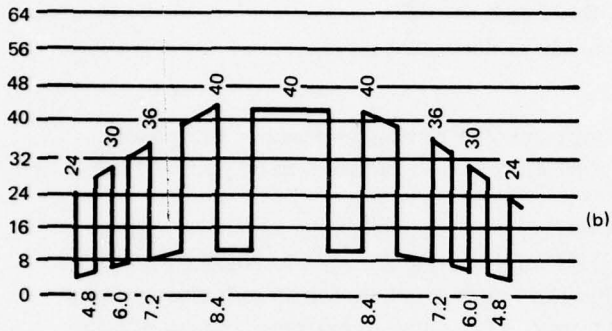
The HIC will now be functionally described with reference to the block diagram in figure A13. The following discussion pertains to an imager configuration of four channels at 21 megapels per second per channel. Only single-channel operation will be described and shown.

The HIC receives commands to operate in its several modes via the GPIB (IEEE 488 interface).

To acquire calibration data, the ICAS is configured to accept lines of captured data while the imager is scanning the white standard. The HIC is sent a command to bypass its normal correction function and to multiplex the incoming digital video data directly to its output. The HIC contains a level translator for converting the balanced-differential ECL signals received from the A/D converter to TTL levels during this acquisition.



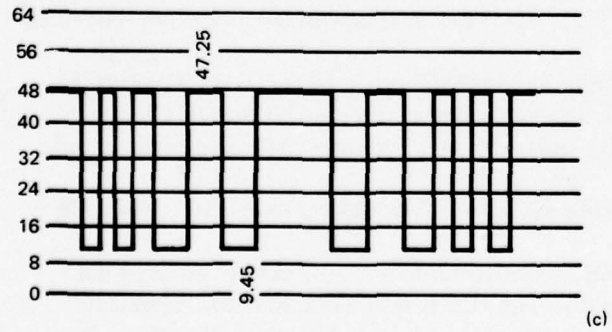
STEP 1. RUN CALIBRATION CURVE WITH WHITEST MATERIAL. STORE SEQUENTIAL VALUES OF REFLECTIVE BRIGHTNESS.



STEP 2. RUN ROUTINE COPY DATA. ACQUIRE SEQUENTIAL VALUES OF REFLECTIVE BRIGHTNESS.

$$\text{COMPUTE } C = 63 \times \frac{\text{COPY B}}{\text{CALIB B}}$$

STEP 3. DIVIDE THE COPY BRIGHTNESS VALUES AS RECEIVED BY THE STORED CALIBRATION VALUES. MULTIPLY BY CONSTANT = 63 AND PIPELINE OUTPUT TO PRESTORAGE PROCESSOR OR FRAME-STORE MEMORY.



STEP 4. STORE, PROCESS, ANALYZE, AND/OR DISPLAY CORRECTED RESULTS.

Figure A12. Illumination correction.

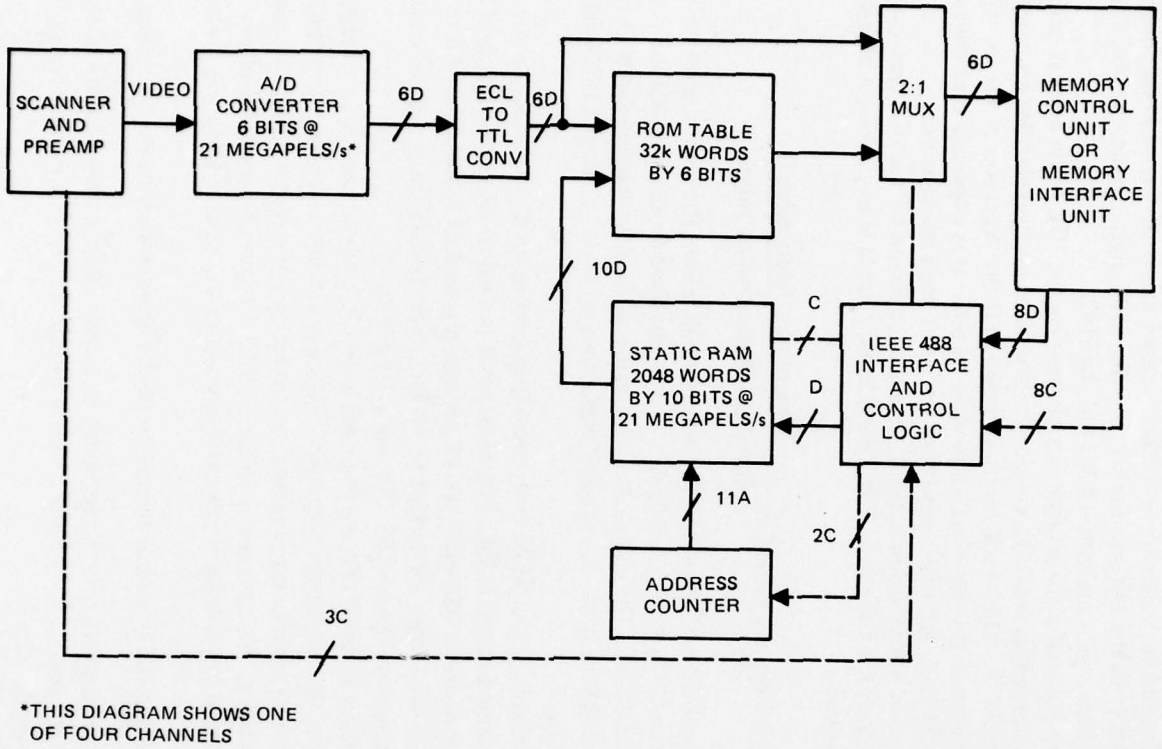


Figure A13. Hardware Illumination Corrector block diagram.

A single sample of a line-scan profile or more probably an average of a number of such samples will be accumulated in the MCU. If a number of samples are taken, they are averaged to form a composite profile of the system response to the white standard target.

At this time a second mode signal is sent to the HIC via the GPIB. In this mode, the process of sending uncompensated digitized video data to the MCU is discontinued. The ICAS is then configured to transmit the 1700 averaged values of the standard brightness profile from the MCU to the HIC via the GPIB. The 1700 digital values are stored in sequence in the random-access memory (RAM) of the HIC.

The transmission of a third mode signal converts the HIC to its normal operating mode, and the equipment is ready to correct for illumination irregularities on copy samples received from the LDTB. The block diagram shows that the precision of the averages of the standard illumination profile is maintained at 10 bits. It is expected that fewer bits (7 or 8) will be sufficient, but conclusive tests have not been made as yet.

The process of illumination correction is accomplished by use of a read-only memory (ROM) lookup table. The function of the ROM lookup table is to provide a high-speed solution to the equation:

$$\text{Compensated output value } C = \frac{63 \times \text{incoming video value}}{\text{stored calibration video value}}$$

Rather than performing the actual division and normalization, the 6-bit digital value of a pel and the corresponding "n"-bit calibration value obtained from the RAM are presented as an address to the ROM. The calculated 6-bit value of the corrected result is obtained directly from the ROM output. A partially populated table of the stored ROM values is shown in figure A14.

The dimensions of the ROM table are dependent upon the accuracy of the calibration averages contained in the RAM. For example if the values of correction data are carried at 6 bits, then the ROM will have 12 address bits and its dimensions will be 4096 words by 6 bits. If the values are carried to 10 bits, then 16 address bits will be required and the ROM dimensions become 65 536 words by 6 bits.

No alterations to the ROM are required unless it is desired to modify the system transfer function of the amplitude response. This may be desirable in order to tailor the amplitude function to provide nonuniformity corrections to a display, printer, or logarithmic function generator. No alterations to the RAM are required unless the power is interrupted (because the RAM is volatile) or a component in the optical system is replaced or altered.

To summarize the complete operation of the illumination correction procedure:

1. The average brightness profile for the calibration is stored in the static RAM at 10-bit (maximum) precision. This brightness profile will remain in memory until a recalibration is required.

2. Routine USPS copy is then input by the system. Values of the digitized image data and corresponding values of the stored calibration curve are applied to the ROM address input on a pel-by-pel basis.

3. Using the data as address inputs, the ROM provides a 6-bit corrected pel output for further processing.

CALIBRATION VALUES

INPUT VALUES	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
63	63																															
62	62	63.0																														
61	61	62.0	63																													
60	60	61.0		63																												
59	59	60.0			63																											
58	58	58.9				63																										
57	57	57.9					63																									
56	56	56.9						63																								
55	55	55.9						61.9	63																							
54	54	54.9						60.8		63																						
53	53	53.8						59.6			63																					
52	52	52.8						58.5				63																				
51	51	51.8						57.4					63																			
50	50	50.8						56.2						63																		
49	49	49.8						55.1							63																	
48	48	48.8						54.0								63																
47	47	47.8						52.9									63															
46	46	46.7						51.8										63														
45	45	45.7						50.6											63													
44	44	44.7						49.5												63												
43	43	43.7						48.4													63											
42	42	42.7						47.2														63										
41	41	41.7						46.1															63									
40	40	40.6						45.0																63								
39	39	39.6																							63							
38	38	38.6																								63						
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34	34	34.6																												63		
33	33	33.5																													63	
32	32	32.5																														63
31	31	31.5																														
30	30	30.5						33.8																								
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10	10	10.2						11.																								
9	9	9.2																														
8	8	8.1																														
7	7	7.1																														
6	6	6.1																														
5	5	5.1																														
4	4	4.1																														
3	3	3.0																														
2	2	2.0																														
1	1	1.0																														
0	0	0.0						00.0																								

ALL VALUES ABOVE
63 ARE INVALID

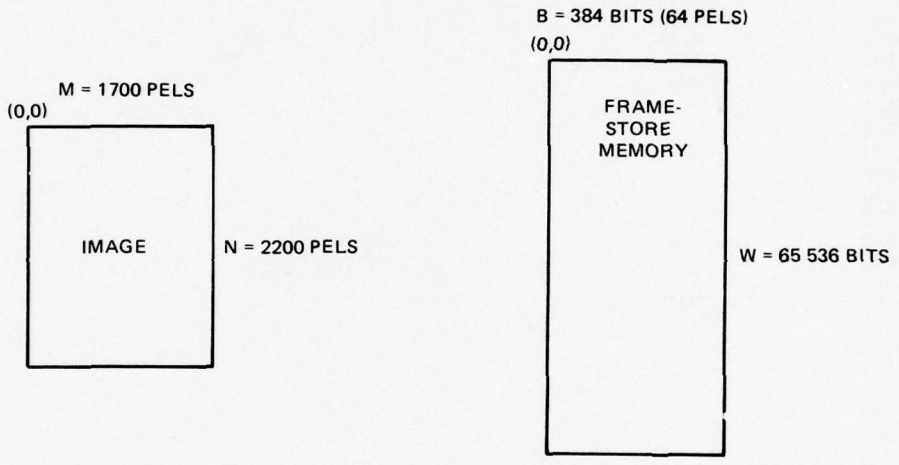
$$C = 63 \times \frac{\text{INPUT VALUE}}{\text{CALIBRATION VALUE}}$$

Figure A14. Calculation of ROM table values.

PERSONALITY CHASSIS

The objective of the ICAS is to store and retrieve digital images. In order to retrieve an image, and not random data, from memory, each video pel must be stored in a known location. In other words, the video information must be formatted (in memory) in a fixed geometric pattern that is compatible with an output reproduction scheme. The storage data structure has been optimized to simplify the retrieval and display problems. Therefore, some input conditioning is necessary to accommodate different types of image scanning equipment.

The video image can be considered to be a matrix of video samples of M X N dimension, where M is the number of pels per line and N is the number of lines. The memory system is a different matrix of storage locations of dimensions B X W where B is the number of bits per word and W is the number of words. Also, one pel requires 6 bits and one FSM word equals 384 bits (64 pels).



Because the memory system has significant access and cycle times, and high-speed operation is required, the best retrieval scheme is to read sequential words, each containing 64 adjacent video pels. In hardware, the first video sample ($v_{o,o}$) of an image is stored in the low-order 6 bits of memory base address (W_b), and the entire image is stored by simple incremental indexing through image and memory matrices.

This data storage scheme is most efficient when the scanning equipment produces a simple noninterlaced rectangular scan of the image. In this case, a scanner-dependent personality module performs a simple demultiplexing operation to pack 6-bit pels into 48-bit words. Each word is stored through a direct memory access (DMA) write operation at the memory cycle rate. The storage addresses are generated by a simple up-counter starting from a base address. When scanner equipment produces a video data stream in a scrambled or partitioned format or divided into two or four separate channels, a special personality module and/or special address calculations are required to reorder the video samples in memory.

The block diagram of the personality chassis is shown in figure A15. This chassis is divided into four functional areas such that, by adding new personality logic cards or replacing the existing ones with a different set, a variety of scanning schemes can be accommodated.

In the simplest case, the scanning hardware provides a single 6-bit data stream consisting of consecutive lines of video starting at the upper left corner of the subject image. These data are received via balanced-differential twisted-pair ECL transmission lines and demultiplexed to 48-bit words containing eight pels each. After conversion to TTL logic levels, the 48-bit data words are sent to line drivers for transmission to the MIU (unscrambling is not necessary because the video samples are transmitted sequentially). As an option, the most-significant-bit (MSB)-only circuit may be selected, thresholding the data at the value 32 and sending a black-and-white-only image to memory.

More complicated situations occur when the scanner hardware sends multiple-channel video to the personality chassis (PC). In one example (fig A16) two Fairchild CCD131 chips are used to generate four video channels. Each chip provides half of each scan line to form a left/right division of the image. Also, each chip has two channels, one for odd-numbered and one for even-numbered pels. The video pels are separated and formatted in the PC, and the appropriate left-half and right-half addresses are generated in the MIU hardware.

In the RCA TDI imager scanning scheme, four video channels similar to those in the previous case are presented. However, in one mode the left and right sides of the image are scanned from the edge toward the center. The formatting and addressing strategy is shown in figure A17. The PC and the MIU cooperate to demultiplex, unscramble, and store the video in a manner such that no gap exists at the center of the image. Since the chip scans 748 pels per line, the storage requirements are twelve 384-bit words per video line with 20 unused pel positions. These blank pel positions must be placed at the ends of each video line in order to avoid a gap in the center of the image when the stored data are retrieved. This is accomplished in the PC by placing two blanks and six pels in memory module 2 address a_1 and in the MICC by storing eight blank pels in memory module 1 address a_1. This arrangement is symmetrical about each line as shown in figure A17 (addresses a_1 and a_{12}).

The personality chassis has been designed with the maximum possible flexibility in order to accommodate other scanning formats without major hardware changes. Four empty card slots are available for additional personality modules. Alternatively, the existing four-card set can be replaced with a card set tailored to a different scanner.

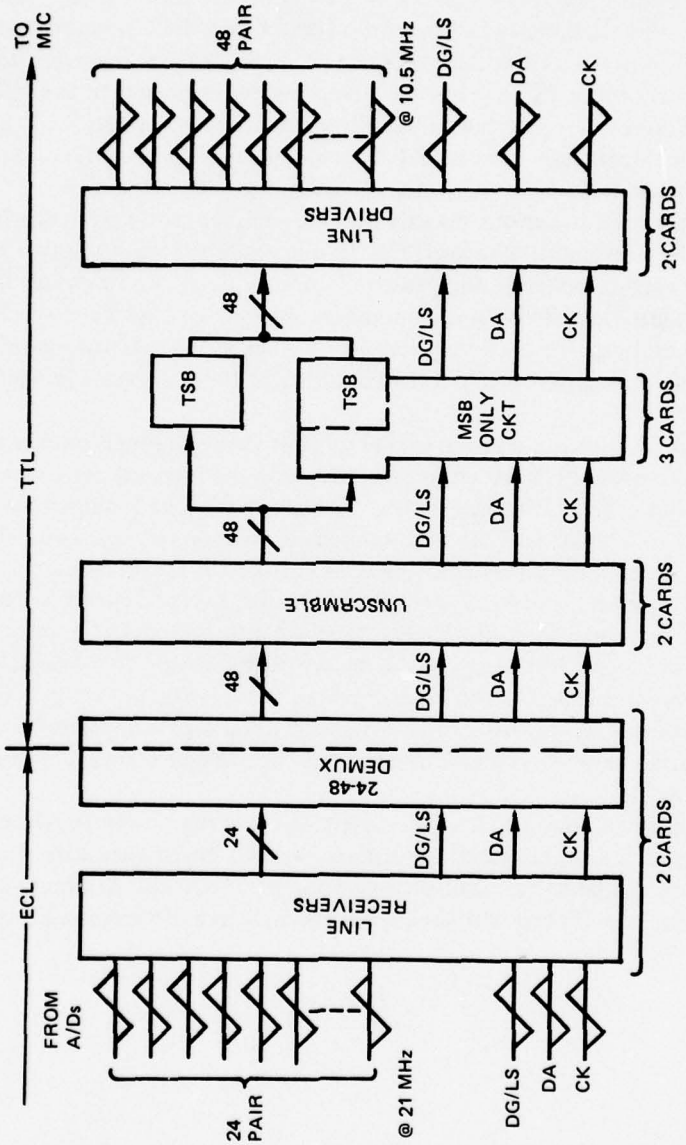


Figure A15. Personality chassis block diagram.

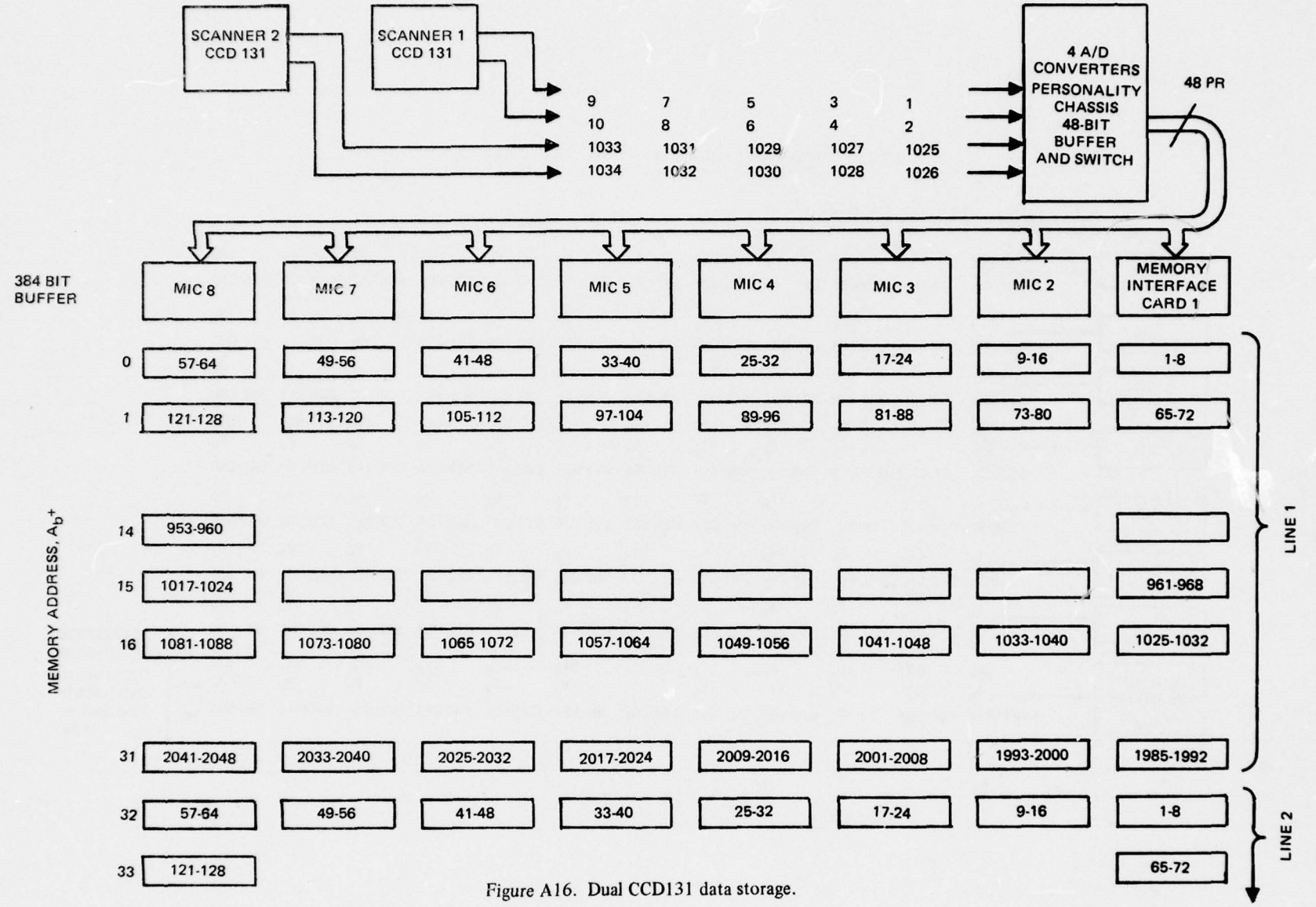


Figure A16. Dual CCD131 data storage.

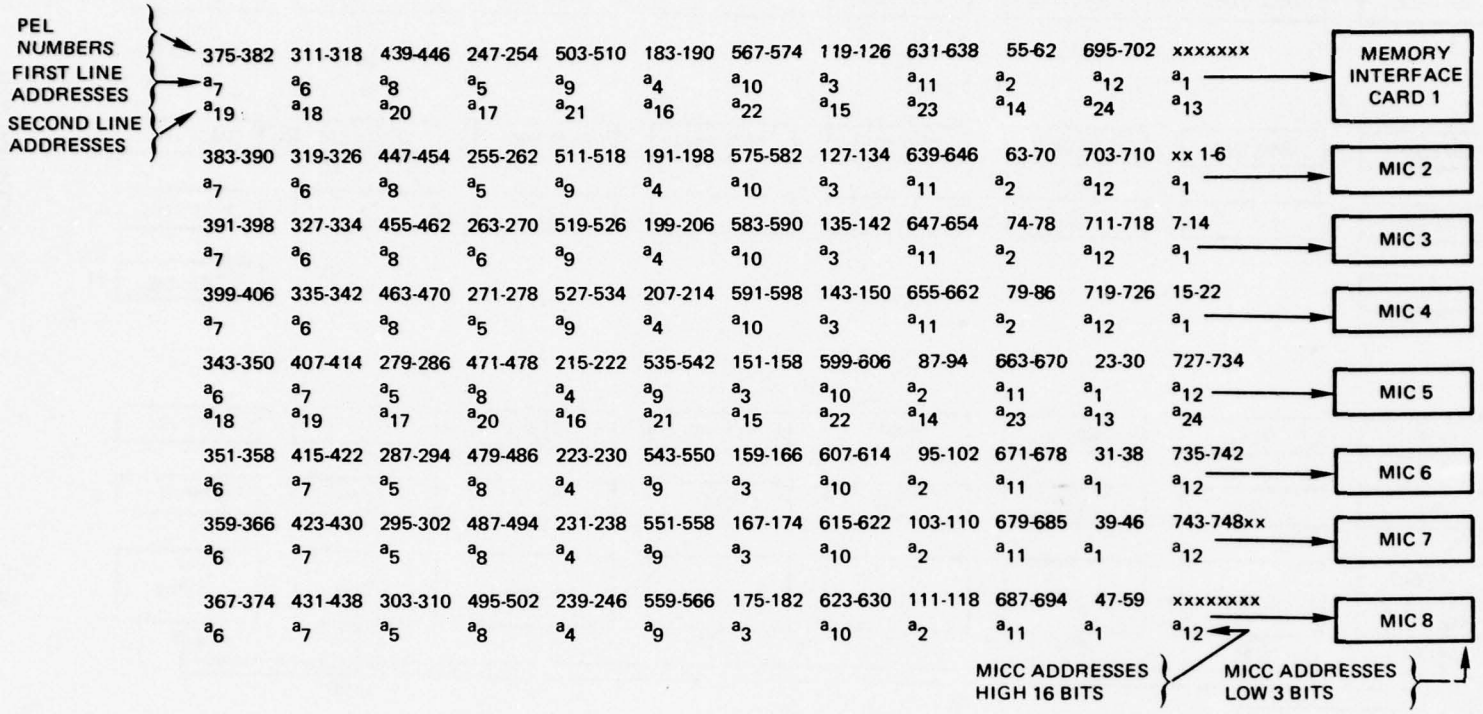


Figure A17. Storage of one video line—RCA TDI chip.

MEMORY SUBSYSTEM

INTRODUCTION

Postal Service goals require the acquisition of image data at the rate of 84 megasamples per second. Previous investigations at NOSC have led to the conclusion that 2^6, or 64, video levels are adequate for the acquisition and display of continuous-tone images. The product of the 84 megapels per second times the 6 bits per sample defines the input data rate for the frame-store memory at 504 megabits per second.

Although not a conclusive fact for this program, previous work at NOSC has indicated that a resolution of 200 by 200 pels per square inch in the original image is adequate for continuous-tone photographs. This yields a requirement for a storage capacity of 40 000 pels per square inch. When multiplied by 6 bits per pel, the required storage capacity becomes 240 000 bits per square inch. Therefore, a total capacity of 22.44 megabits will be required to store the total image data for an 8½-by-11-inch page of copy.

The high input data rate is not compatible with practical memory devices so a speed versus word width tradeoff is required. In order to utilize readily available hardware, the video data must be demultiplexed from 6 bits per pel to some number (n) pels per memory word. This results in a digital word rate that is consistent with realizable, low-risk memory systems. Demultiplexing is accomplished by saving n consecutive video samples ($n > 1$) in a register of length equal to 6 n bits (6 bits per pel). The resulting data words can then be handled by subsequent logic at 84n megawords per second. For example, if n=2, then the 84-megapel-per-second video data would be converted to 42-megawords-per-second data with each word containing two pels, or 12 bits. The eventual choice of a value for n is determined by the video rate and the available memory cycle times.

When the first memory module (64k words times 48 bits) was procured, the state-of-the-art memory device was an MOS dynamic RAM organized as 4k words by 1 bit. The operating speed of the typical 4k memory chip was in the 600-900-nanosecond range, with faster chips available at premium cost. An additional factor to be considered in selection of a memory system architecture is the fact that industry offers off-the-shelf basic memory systems organized with word widths in multiples of 8 bits. Table A1 shows how an increase in the multiplex ratio to 64 produces a memory system 384 bits wide and achieves the required speed reduction with available devices. The complete memory system is therefore 64k words by 384 bits with acceptable read/write cycle times of approximately 750 nanoseconds. This memory is packaged in 42 (vertical) inches of a 19-inch rack, including power supplies. The current cost of such a memory system (at approximately 0.5¢ per bit) is about $125 000.

TABLE A1. EFFECTS OF MULTIPLEX RATIO n.

Multiplex Ratio	Word Width, bits	Memory Frequency, MHz	Word Clock Period, ns
1	6	84	11.9
2	12	42	23.8
4	24	21	47.6
8	48	10.5	95.2
16	96	5.25	190.5
32	192	2.62	381
64	384	1.31	762

The full frame-store memory system can be conveniently modularized into eight separate units. The ratio n then equals eight for a single memory module and eight modules form a complete system (n=64). The interfacing, control, and generation of the memory system becomes a manageable set of problems despite the large word width.

Figure A18 shows how the multiplex ratio and modularization produce a system with a significant number of identical units. Also shown in figure A18 is the amount of versatility afforded in accommodating different sources of video input. Scanner hardware can input data to the memory at line A, B, C, or D as required. The only hardware affected by a new scanner is the appropriate personality module plus, in some cases, the Memory Interface Control Card (MICC).

The memory module is a 64k-word by 48-bit self-contained memory subsystem. It performs the basic read and write operations over an interface designed for high reliability. The interface is described in terms of the MCU; however, its features and principles apply equally to operation with the Memory Interface Unit (MIU) or any similar equipment.

THE MEMORY INTERFACE

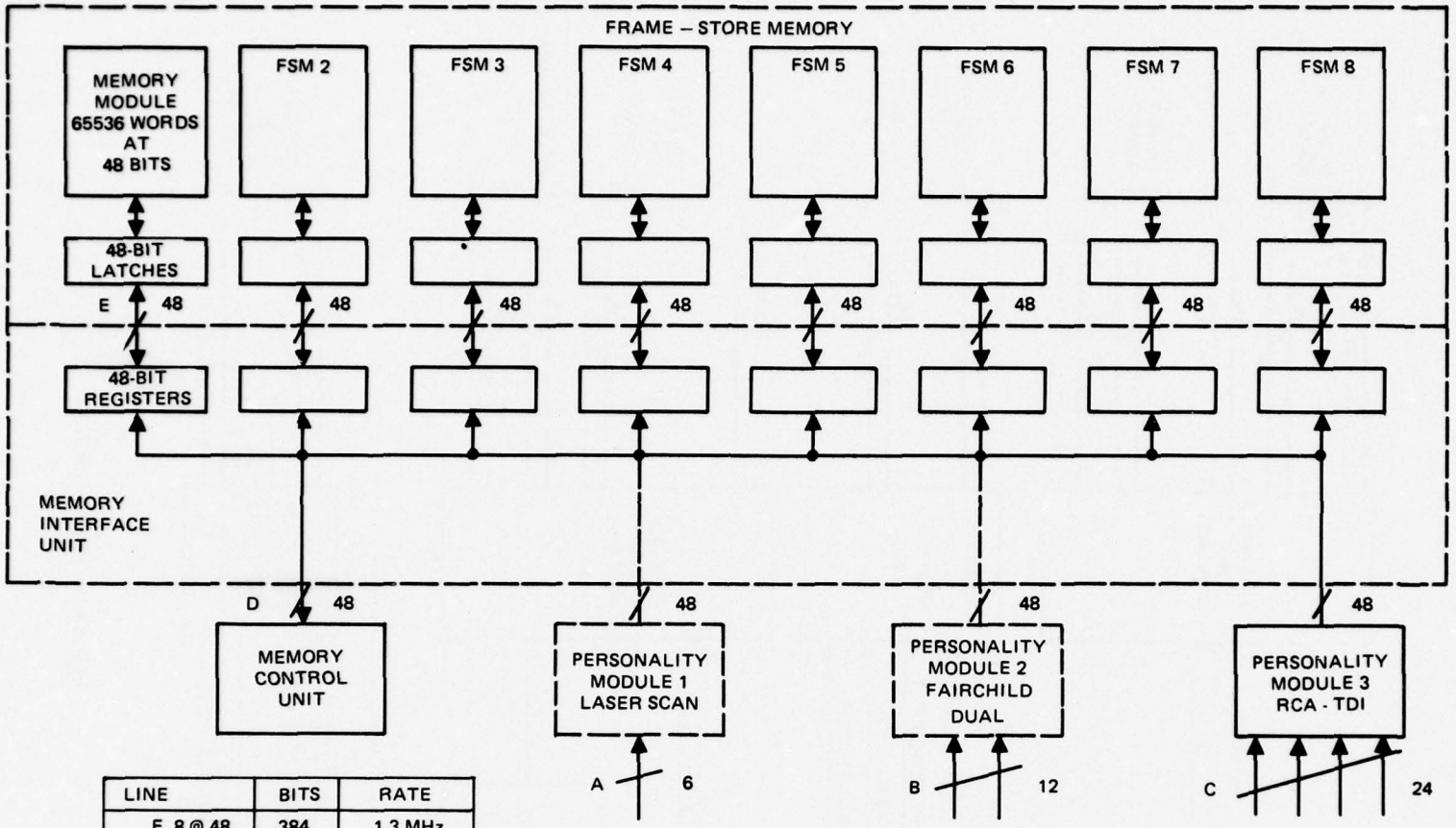
The memory interface logic is divided into four basic parts (fig A19): address input to the memory, data transmission to and from the memory, command lines to the memory, and status information from the memory. All signals associated with the memory are transmitted over differential twisted-pair lines. High common-mode rejection and a 15-volt common-mode range of the twisted-pair line drivers, receivers, and transceivers (75114/115/117) provide for highly reliable data transfers.

The address information is generated in the central processing array and is presented to line drivers via the Memory Address Register Bus (MARB). The address information is actually divided into two parts. One part is a 16-bit address field selecting any one of the available 64k memory words. This address specifies either the read or the write location in memory. In addition, six independent BYTE SELECT lines are provided which may selectively enable or disable the write operation on any combination of the 8-bit bytes in the selected word. The BYTE SELECT inputs do not affect read operations.

The 48 data bits are transmitted to and from the memory over a common 48-pair cable. Forty-eight twisted-pair transceivers operate in much the same way as the twisted-pair driver/receivers used for the memory address and command lines. The only difference in the memory data lines is that they operate in half-duplex mode; that is, data transmission occurs in both directions (to and from the memory) over the same lines but not at the same time.

There are five control signal input lines associated with memory. These are the READ, READ ENABLE, WRITE, and REFRESH REQUEST commands and the REFRESH MODE control line. The memory system responds to input commands with one of four status or control replies – DATA AVAILABLE, CYCLE COMPLETE, BUSY, or REFRESH BUSY. These commands and status lines are used in various ways to accomplish one of the three possible memory functions (read, write, or refresh). Figure A20 details the relative timing between the memory command, address, data, and status reply.

The read operation is performed by simply transmitting the appropriate memory address to the memory and initiating a read command pulse. The memory system responds with a BUSY signal while the memory itself performs the function and waits for required



LINE	BITS	RATE
E 8 @ 48	384	1.3 MHz
D	48	10.5 MHz
C	24	21 MHz
B	12	42 MHz
A	6	84 MHz

Figure A18. Full Frame-Store Memory

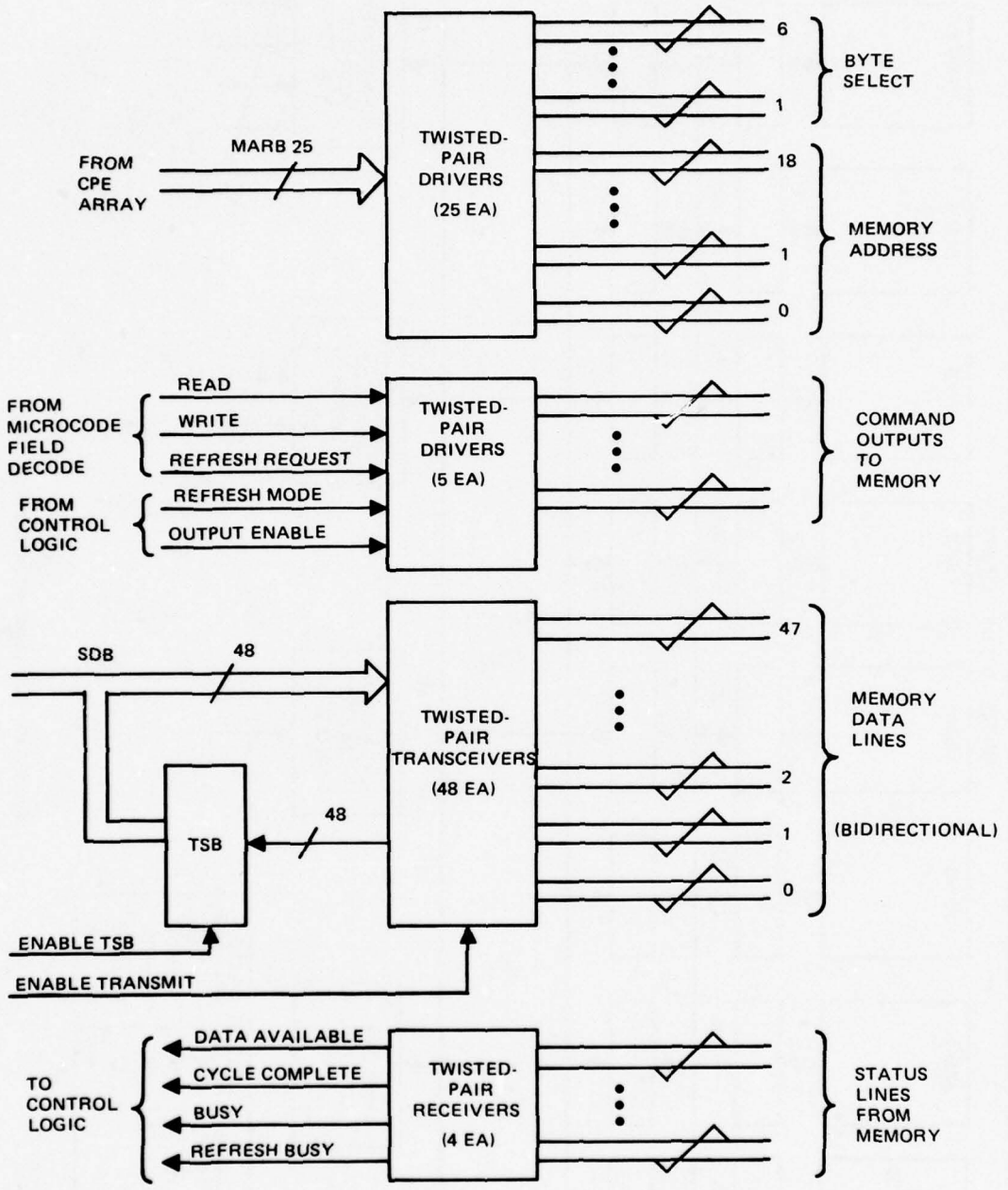


Figure A19. Memory interface.

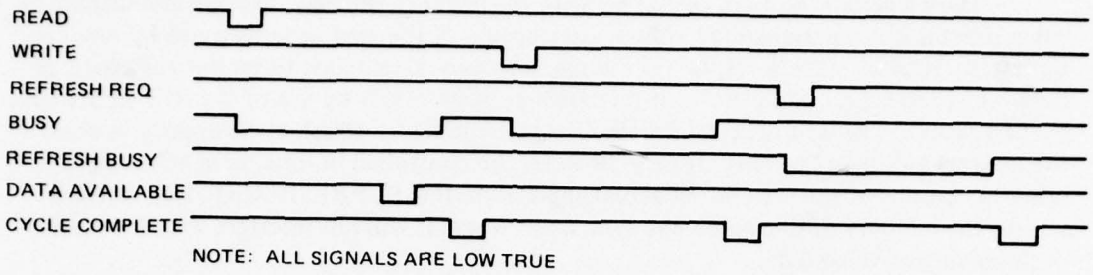


Figure A20. Memory timing.

propagation delays. After the access delay, the data from memory are available on the 48-bit data bus. The memory responds with a DATA AVAILABLE pulse, at which time the memory interface tristate buffers may be enabled to the controlling device. The time/delay or propagation delay from initiation of the READ command until the memory responds with the data and the DATA AVAILABLE pulse is approximately 450 nanoseconds. The memory system, however, is not yet ready to accept another command. The BUSY line remains true for another 200 nanoseconds because of internal propagation delays in the memory system. When BUSY is removed, the CYCLE COMPLETE pulse is sent by the memory indicating that the present cycle has been completed.

It is convenient that the memory system contains its own 40-bit data register. This permits the MCU to return at a later time (provided a subsequent read or write operation has not been performed) and simply reenable the same data word through the memory tristate buffer. It is not necessary to generate another address and READ command. This feature is important to larger systems which use more than one memory module. A type of interleaving is possible which effectively eliminates the read access delay in some cases.

In the write operation the address must be presented to the memory as in the read operation. The data to be written into memory must also be presented. The write operation is initiated by a WRITE pulse. The six 8-bit bytes of a memory word may be individually enabled during the write operation by use of the BYTE SELECT lines; any byte not enabled may not be written into. The response of the memory system to a write operation is identical to the response to a read operation.

Since the memory system is constructed from dynamic MOS memory chips, the data within the memory are volatile and must be refreshed on a periodic basis. The entire memory system must be refreshed every millisecond. This requires that 64 REFRESH REQUEST signals be sent to the memory every millisecond. The specification for full refresh every millisecond is determined by the worst-case conditions, particularly at elevated temperatures. In a controlled-temperature environment this specification may be relaxed considerably.

The memory system may be refreshed in two different ways. If desired, the refresh requirement can be met by the memory system itself with its own internal logic. With the REFRESH MODE signal in the appropriate state the memory system generates refresh requests on a periodic (but asynchronous) basis and satisfies the minimum refresh requirements. During automatic refresh the memory system disallows any READ or WRITE commands attempted during the refresh cycle. A signal called REFRESH BUSY is transmitted by the memory system during refresh operations to inform the control hardware that the memory is not available because of refreshing. The timing of the refresh cycle is approximately the same as that of a read or write cycle.

During certain types of operation with the memory (namely, capture and display of video data) it is not permissible to allow interruption of the read or write cycle by automatic refresh. During such times the refresh mode control is switched to inhibit automatic refresh. The refresh requirement must then be met by the MCU by use of the REFRESH REQUEST signal. The REFRESH REQUEST signal initiates a refresh cycle exactly as does the internal automatic refresh. It may, however, be controlled in time, or synchronized to other operations of the system. In actual application this REFRESH REQUEST signal is sent to the memory during video line sync times where it will not interfere with the storing or displaying of video data.

MEMORY INTERFACE UNIT (MIU)

INTRODUCTION

In the pre-FY77 system configuration, the MCU was the only hardware that communicated with the memory subsystem. Because only one memory was involved, the necessary input/output and control logic could easily be contained within the MCU. In addition, video data from the scanning logic were demultiplexed in the MCU. The result was that all data transfer logic to and from the memory was implemented in one chassis.

The FY77 system expansion increases the memory capacity from one module to eight, and new scanner hardware provides up to four video input channels. This increase from 3.14 million bits to 25.16 million bits and from a single data channel to four data channels cannot be accommodated in the existing MCU enclosure. Therefore, a separate Memory Interface Unit (MIU) is being added. The new unit will act as a traffic controller to route data between the memory modules and the remainder of the system hardware. In addition, it will perform a direct memory access (DMA) control function to route scanner data directly to the memories and avoid the time delay necessary in the MCU.

The video demultiplexing function (previously performed in the MCU) will now be done in a completely separate chassis (the PC). The video input from the new four-channel scanners is increased from 6 bits to 24 and the output to the memories from 48 bits to 384.

The MIU must perform two fundamental functions. First, the MCU must have access to any of the eight memory modules in such a manner as to provide software upward compatibility. This implies that the new eight-module configuration should appear to the MCU as a 512k-word by 48-bit system. Second, the scanner data must be stored at an effective input rate of 84 megapels per second; therefore, the memory must appear to the scanner video input hardware as a 64k-word by 384-bit system. This configuration change is implemented dynamically in the MIU.

HARDWARE CONFIGURATION

The MIU is a card cage which occupies 20.75 vertical inches of a standard 19-inch rack. The MIU is partitioned into a control function (two cards) and a data handling function (eight cards). The control cards are 8½-by-15-inch wirewrap panels with a capacity of about 200 chips. The eight identical memory interface cards (MICs) are custom, two-sided printed-circuit cards, each containing 123 chips. The cards plug into a standard wirewrap

chassis from the rear of the rack. Connection is made to the backplane by three 108-pin connectors on one card edge for a total of 324 pins. The opposite side of the card has two additional connectors which are used for the FSM module interface cables. This card, therefore, has a total of 540 I/O pins. The chassis is secured to a slide-mounted fan box which cools the card cage and provides access for test and maintenance. The chassis is oriented so that the backplane wiring is accessible from the front of the rack. The interface cables plug directly onto the cards from the rear of the rack. The interconnect scheme (shown in fig A21) connects a total of 1530 wires to the MIU via 10 cables.

CIRCUIT FUNCTIONAL DESCRIPTION

The printed-circuit memory interface card (MIC) is shown in figure A22. The function of this card is to route data, address, and control signals between a memory module and a data source or sink. One interface card is provided for each memory module. The MIC contains the following elements:

1. Twisted-pair line receivers and line drivers for all I/O signals
2. A 48-bit input data register
3. Tristate data I/O multiplexing
4. Provision for adding high-speed data output

The functional capability of the MIC is as follows:

1. Write a 48-bit word to any of the eight memory modules. The memory system is therefore configured to be 512k words by 48 bits operating at speeds approaching 1.5M words/s (12 megapels per second).

2. DMA Write. Write eight 48-bit words (384 bits total) to all memories simultaneously. The memory system is then configured to 64k words by 384 bits, which achieves a pel input rate approaching 96 megapels per second.

3. DMA Read. Expansion capability to achieve a high-speed parallel data output.

The two memory interface control cards (MICCs) contain sufficient hardwired logic to direct the operation of the MICs, resolve conflicts between memory users, maintain proper interface timing, and control the DMA write operation. Figure A23 is a block diagram of the MICC function. Operation of the MICC can be divided into two categories. One involves normal data interchange between the memory controller and the individual memories (one at a time) and the the other is the DMA write operation (scanner data to memory).

When the ICAS is operating under normal program control, 48-bit data and instruction words are transmitted between the MCU and one of the memory modules. Because the configuration is 512k words by 48 bits, 19 address bits are required to select a single memory location. These 19 address bits are divided into two groups. The high-order 16 bits select a word within a memory module, and the low-order 3 bits select the module. There are two particular advantages to dividing the address bits in this way when read operations are being performed. The first advantage is called "graceful degradation"; that is, the system can still operate, but at reduced speed, even with the loss of memory modules. The second advantage is that in some cases the read access time can be eliminated.

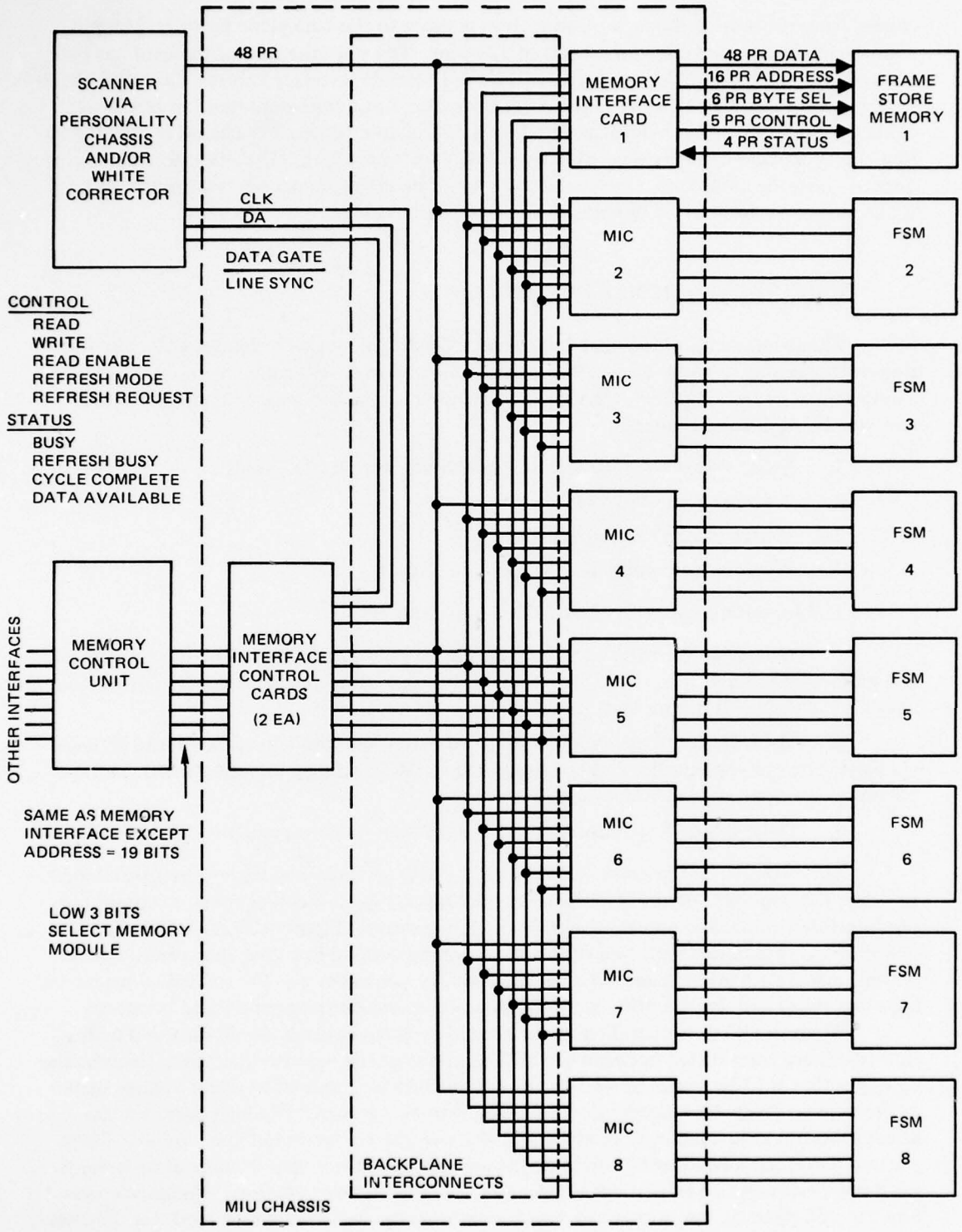


Figure A21. Memory Interface Unit.

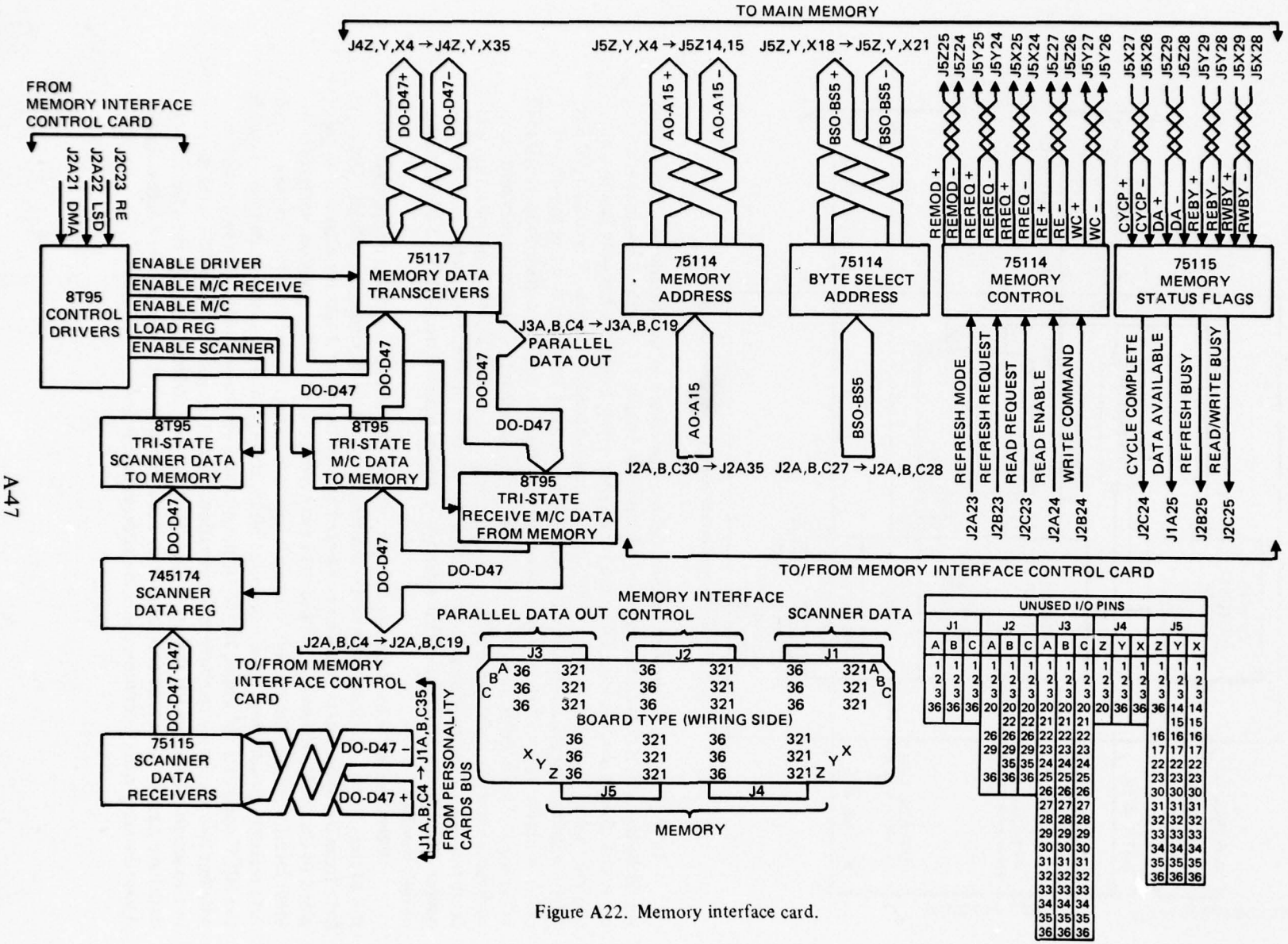


Figure A22. Memory interface card.

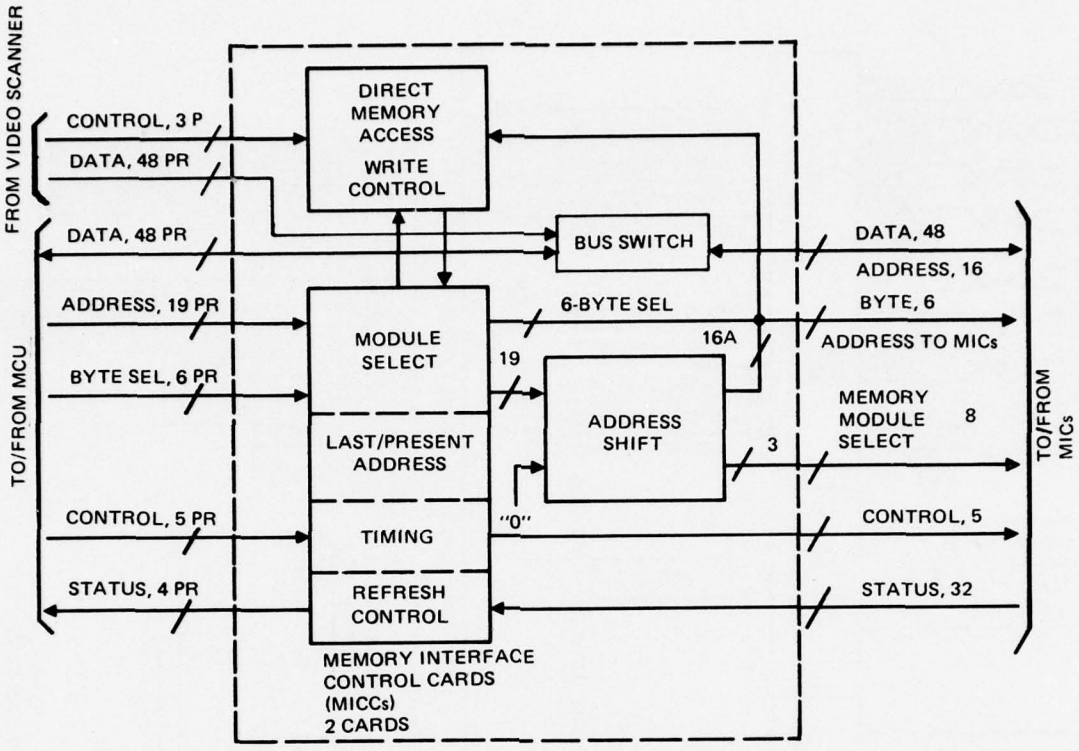


Figure A23. Memory interface control card block diagram.

In the event of a memory module failure, one-eighth of the program and image data would be lost. If, however, the memory address is shifted left 1 bit, the low-order address bit would always contain a 0. The memory module-select field then has only 2 active bits and may select between any one of the four even-numbered memories. A second 1-bit left-shift would restrict access to memories 0 and 4, and a 3-bit shift would select memory 0 only. A hardware overflow test ensures against attempts to read or write into memories not being used. This type of memory address shifting is completely software-transparent, since address integrity is maintained in the low-order bits. Of course, a system initialization and bootstrap operation must be performed after the number of memories is changed. The apparent effect to the MCU is that the memory system is reduced from 512k to 256k, 128k, or 64k words.

When the MCU has requested a read cycle (either instruction fetch or operand fetch), the address (upper 16 bits) and READ command are sent to all memory modules. Only the data from the appropriate module (as selected by the low-order 3 address bits) will be enabled to the MCU. However, all modules have performed a READ operation, each from the same location within the module, and each has stored the retrieved data into its own output data register. In addition, a register on the MICC stores each memory read address. Logic in the MICC compares the upper 16 bits of the previous and current addresses to determine whether two successive memory read operations have attempted to access the same location in two separate modules. If the upper 16 bits of the two addresses match, then the desired data have already been read and there is no need to wait for the memory read access delay. An intervening write operation voids the address match test.

Preliminary estimates indicate that an increase of 10-15% in system throughput could be achieved by this kind of interleaving with the present instruction set. With the addition of 8-10 new non-memory-reference instructions, an additional 10% could probably be realized.

The second operation the MICC must perform is control of the DMA write of scanner video data to memory. After initialization, the MICC takes complete control of the memories by sending a continuous signal to the MCU. The MICs then receive preformatted video information from the personality chassis as well as control, timing, and address information from the MICC. Since the processing capability of the MCU is not available at this speed, hardwired logic on the MICC must generate each memory address. The manner by which the addresses are calculated is determined by the type of scanner and its configuration. Simple single-channel inputs such as the CCD121 need only a simple count or increment. More complicated scanning systems employing multiple channels or multiple devices require dedicated address calculation which includes multiple adders, comparators, and multiplexers.

To achieve the maximum video input rate, each 48-bit input word is stored in a register on the appropriate MIC. When all eight registers have been loaded, a write to all eight memories simultaneously is performed and the next address is calculated and tested. With fewer than eight memories, the same operation occurs, but the maximum rate is reduced. Previous discussion of multiplex ratio has shown the tradeoff between word width and operating speed. During a DMA write operation with eight memory modules, 384 bits can be stored during each memory cycle (t_{mcy}). If a memory failure reduces the memory system from eight to four modules, then only 192 bits can be stored in one t_{mcy}. The effective video input rate is, therefore, divided by 2.

MONITOR-DISPLAY UNIT

The monitor-display unit (fig A24) accepts digital video from the MCU for the purpose of displaying images stored in the frame-store memory. Six-bit video pels are sent to a D/A converter located adjacent to the display. Raster sync is maintained by independent horizontal and vertical drive signals. The timing is completely controlled by a microcode routine in the memory controller. Suitable level translators are packaged adjacent to the D/A converter to provide the signals required by the monitor.

The Conrac RQB monitor is unique in that it does not require EIA or composite video for synchronization. The monitor's raster is driven by internal phase-lock loops which will accept a wide range of horizontal and vertical frequencies. Table A2 presents the important characteristics of the RQB Monitor. Figure A25 shows the front-panel controls.

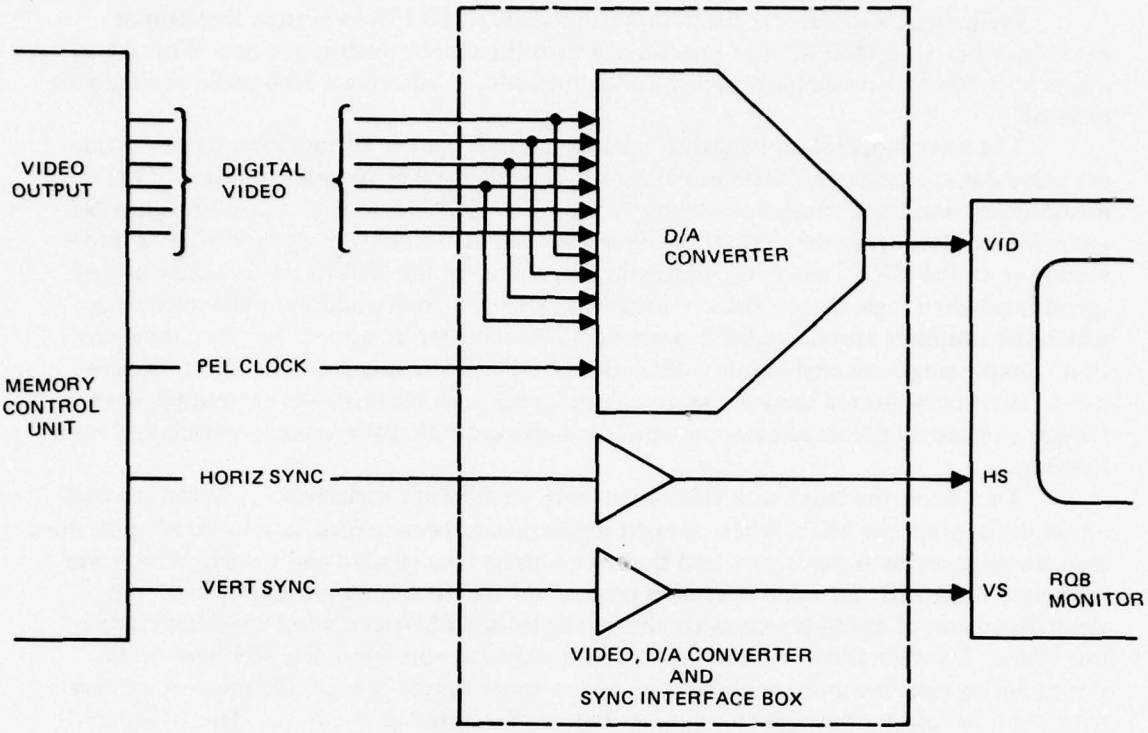


Figure A24. Video output interface.

TABLE A2. CONRAC RQB MONITOR SPECIFICATIONS.

Video bandwidth	±1 dB at 30 MHz; ±6 dB at 40 MHz
Horizontal frequency	15 to 40 kHz
Vertical frequency	15 to 60 fields per second
Display size	14 inches wide by 11 inches high
Input impedance	50k ohms shunted by 10 pF
Phosphor	P-4 (white)

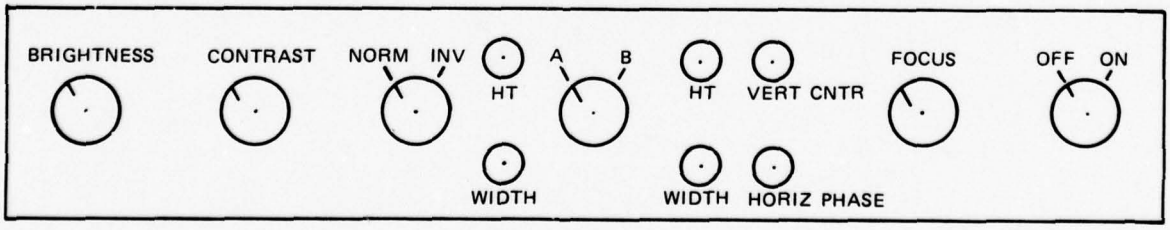


Figure A25. Conrac RQB front-panel controls.

DIGITAL IMAGE ANALYZER

INTRODUCTION

Prestorage processing is an important adjunct to image acquisition for a number of reasons. By definition, prestorage processing includes any intentional augmentation of image data prior to acceptance of the data into the frame storage buffer memory. This processing includes prescanner strategies to determine optimum color of illumination for the main scanner, accumulation of statistical data pertaining to the distribution of reflection densities of the copy, image enhancement algorithms which can be executed in real time without requiring buffer storage, and any of a number of compression techniques which can reduce the final required capacity of the frame-store memory. This section is devoted to a description of a digital image analyzer (DIA) and of its purpose, which is to identify and exploit those parameters of various image types which may be used to optimize the acquisition, storage, and compressibility of the image data.

A diagram of an advanced electronic message input terminal is shown in figure A26. Only those portions pertaining to prestorage processing are described here. As shown in the diagram, 8½-by-11-inch copy is input to the system at a rate of 240 inches per second, or a page rate of 20 pages per second. At the prescan station there are three image sensors—one with red illumination, another with green, and a third with blue. The three colors of illumination will be used for possible contrast improvement and for future color applications.

Each of the three outputs from these sensors is fed into a preamplifier with fixed gain and offset (level). The gain and offset on all three preamplifiers are adjusted so that when black velvet, with the lowest possible reflectance, is placed in front of the image sensors, the resulting output from the preamplifiers will produce an output of all 0's from the A/D converters; and when a white surface of $BaSO_4$, with the highest possible reflectance, is placed in front of the sensors, the resulting outputs from the A/D converters will be all 1's. The weighted, or nonlinear, A/D converters will convert data according to Weber's* rule in order to minimize the total number of bits needed to represent each pel.

The DIA is a statistics-gathering machine used to supply image data to the mail mode selector where various decisions are made to properly set up system controls for the main scanner stations.

The mail mode selector is a decision unit for the main scanner system control. It accepts inputs from the image analyzer and uses them for the following: gain and offset adjustments of the main scanner preamplifiers; selection of enhancement modes, which may be either digital or analog; selection of type of data compression; selection of bit precision; and selection of image resolution. For a complete description of these functions, the reader is referred to reference A2, page A-14.

The DIA in the advanced electronic message input terminal must analyze data at the prescan station from the three image sensors simultaneously. (It must accumulate all types of statistics simultaneously.) The DIA is designed to accumulate the different types of statistics, one at a time, for one input channel. It is designed to accept data at a channel rate of 21 megapels per second. Four or more channels will be required to produce the total 84-megapel-per-second design goal.

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*Not Weber's fraction, but a geometrically proportional step increase for successive grey levels.

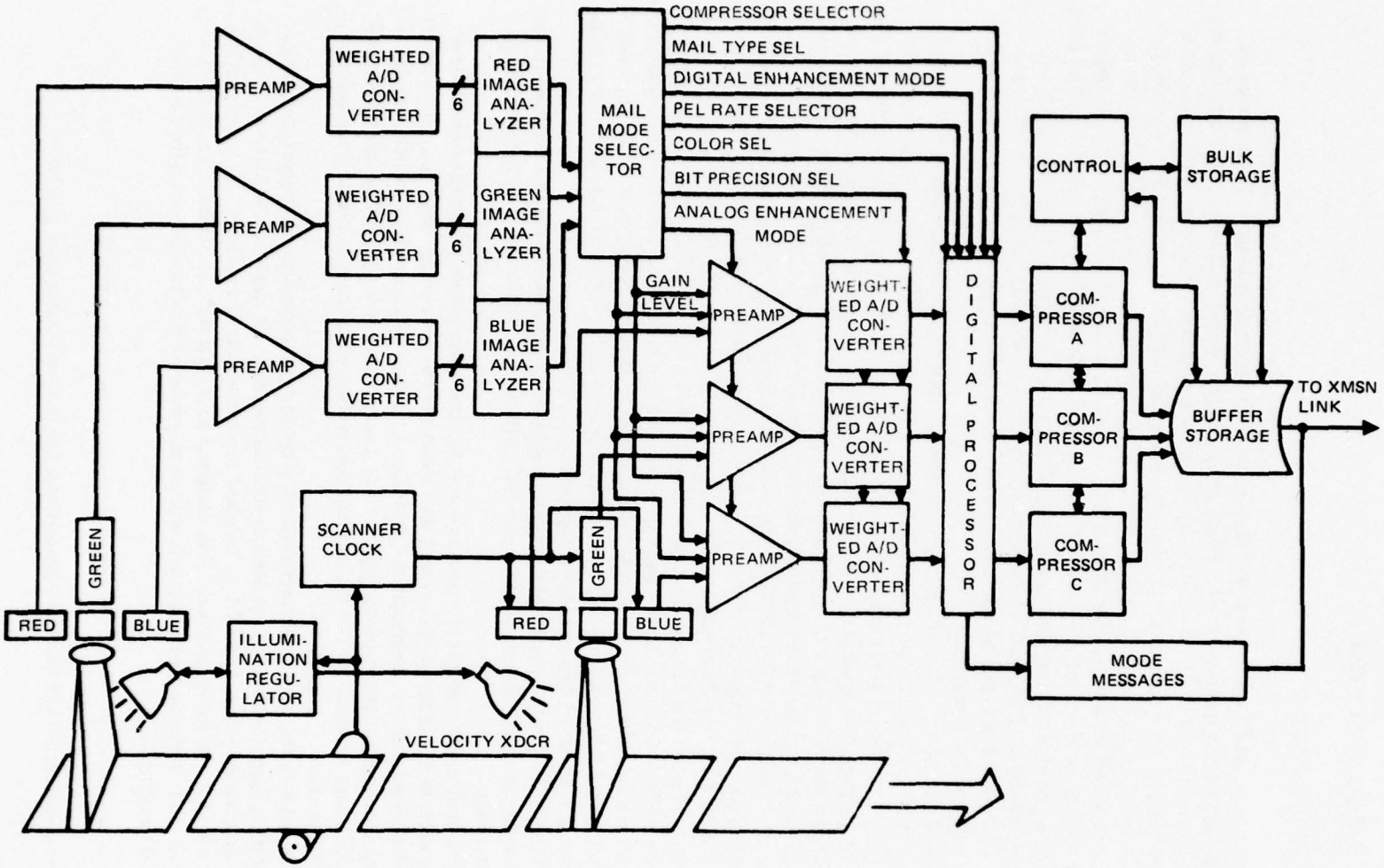


Figure A26. Advanced electronic message input terminal.

GENERAL DESCRIPTION

The NOSC DIA is a 3½-by-19-inch rack-mount unit which is constructed of 10000-series emitter-coupled logic (ECL) on Augat multilayered wirewrap logic planes. The DIA is designed to generate several types of image statistics, in a sequential manner, which include pel brightness statistics (PBS), run length statistics (RLS), and one-dimensional first difference statistics (FDS). There are two interfaces to the analyzer. One is the high-speed image data input port with all inputs ECL-compatible. At present this interface will accommodate image data from the USPS Large Drum Test Bed (LDTB) and the NOSC Video Transmission System (VTS). The second interface is an implementation of the IEEE STD 488-1975 General-Purpose Interface (GPIB). This interface allows operation of the DIA as a peripheral device, with control from the Tektronix 4051 Graphic Display System. A simplified block diagram is shown in figure A27.

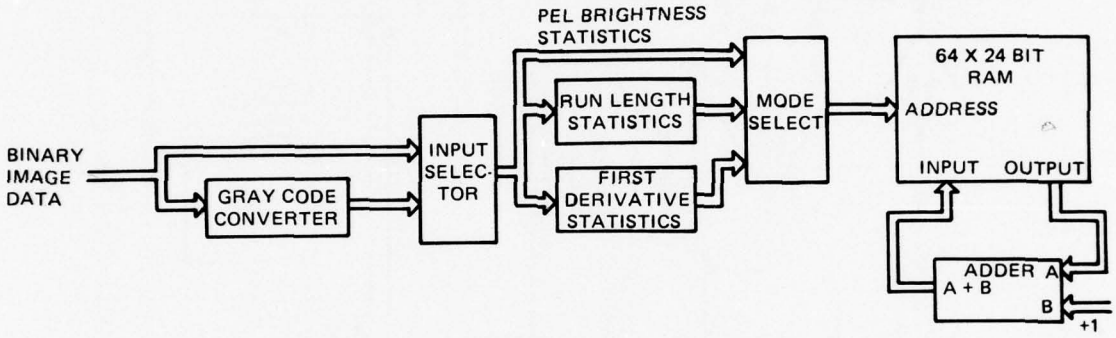


Figure A27. DIA simplified block diagram.

The DIA will generate statistics on any 6-bit input data format. Units currently interfaced with the DIA use a 6-bit binary format. The DIA is capable of converting binary information to Gray code in order to investigate possible improvement in data compression. All subsequent modes discussed allow the use of either binary or Gray code data for analysis.

In the PBS mode the DIA accumulates the total number of occurrences of pels at each of the 64 possible brightness levels throughout an entire image. The upper left portion of figure A28 shows this operation pictorially. Image data from the sensor are amplified and converted to digital format in the A/D converter. The output is a 6-bit binary code, with all 0's representing a black pel and all 1's representing a white pel. This 6-bit code is used as an address to select one of 64 memory locations in the high-speed ECL random-access memory. The contents are read out and incremented by 1 in a high-speed adder and then stored back in the same memory location. This operation is done on a pel-by-pel basis throughout the entire image. The contents of the 64 memory locations are then read out, either manually from an LED display or by a device on the GPIB (MCU or 4051) for generation of a human-oriented display (tabular, bargraph, etc).

In the run length statistics (RLS) mode, the analyzer accumulates totals of either runs of 0's or runs of 1's in specified bit plane of an image. The middle left portion of figure A28 describes this operation. Data output from the A/D converter are fed through a bit plane selector since only one bit stream at a time may be operated on. The output from the bit plane selector is fed into a counter which counts runs of either 0's or 1's depending on the particular

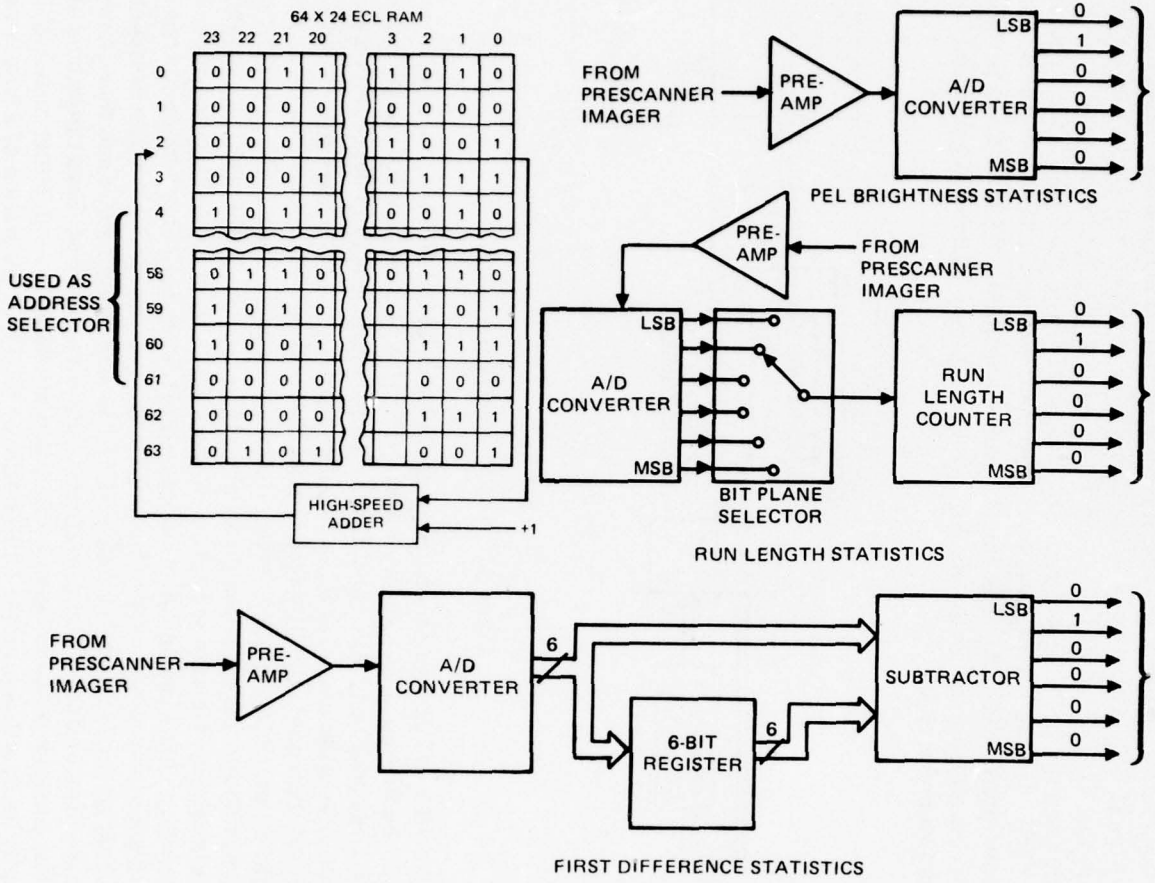


Figure A28. DIA operating modes.

mode selected. At the end of run, the count contained in the 6-bit counter is used as an address to select one of the 64 memory locations as in the PBS mode. There is a 6-bit limitation to the counter, however, which means that runs of length greater than 64 will cause multiple runs to be counted. This is true in the DIA for any run-length-encoding data-compression scheme. For example, for a run of 66, memory location 63 and memory location 1 would each be incremented. Note that run lengths of 1 through 64 correspond to memory locations numbered 0 through 63. In the DIA there are 24 individual modes for the accumulation of run length statistics. There are six bit planes each allowing runs of 0's or runs of 1's. Each of these may be accumulated by use of either the binary code input or Gray code input, resulting in a total of 24 modes.

The first difference statistics (FDS) modes compute the absolute value of the differences between successive pels in an image. The lower portion of figure A28 shows the operation of the FDS modes. Image data from the A/D converter are input to both a 6-bit storage register and a subtractor. The storage register contains the previous pel value, which is subtracted from the present value to obtain the difference. This difference is then used as an address to the 64-location random-access memory as in the previous modes.

There are several other modes of operation for the image analyzer. One of these is the display memory mode. In this mode front-panel switch inputs are used to address each of the 64 memory locations to read out the contents of an 8-digit octal LED display. This information can also be read out through a general-purpose digital interface (the GPIB). Other modes are designed primarily for diagnostics; they include loading one or all memory locations from a manually switched input bus, a clear-memory mode, and continuous-count modes to check the operation of the ALU and data registers.

A more detailed description of the hardware operations of these modes is available in reference A2, pages A-19 to A-24.

CIRCUIT DESCRIPTION

Figure A29 is a more detailed block diagram of the DIA. There are two data sources input to the data source multiplexer, one from the high-speed scanner input port and one from the GPIB interface. The selected binary data are then fed into the input selector (multiplexer) and the binary-to-Gray code converter. The input selector selects either binary or Gray code image data for analysis. The mode selector selects one of the three types of statistics to be accumulated by the analyzer (FDS, RLS, PBS). The output from the mode selector is strobed into a 6-bit pipeline register for data resynchronization. From this register alternate pels are strobed into each of the two 6-bit data registers organized as a ping-pong register with outputs alternately selected by the address selector for reading and writing data into the RAM. After statistics have been gathered, the address selector selects the interrogate address input for reading data out of the RAM. There are two sources for the interrogation address, one from a manual entry from the front panel and the other from the interface. The last input to the address selector is from a control counter which is used for clearing the memory and also for diagnostic purposes. The 64-word by 24-bit RAM is used for accumulation of statistics. The data multiplexer selects data from one of three sources for input to the READ DATA register. They are the RAM output data, the WRITE DATA register output, and an external 24-bit input bus, which currently is controlled by a series of switches. Data stored in the READ DATA register are input to the arithmetic logic unit (ALU), the LED display, and the GPIB interface. The ALU is capable of performing 32 arithmetic and logic functions on pairs of 24-bit words. The WRITE DATA register stores the output information from the

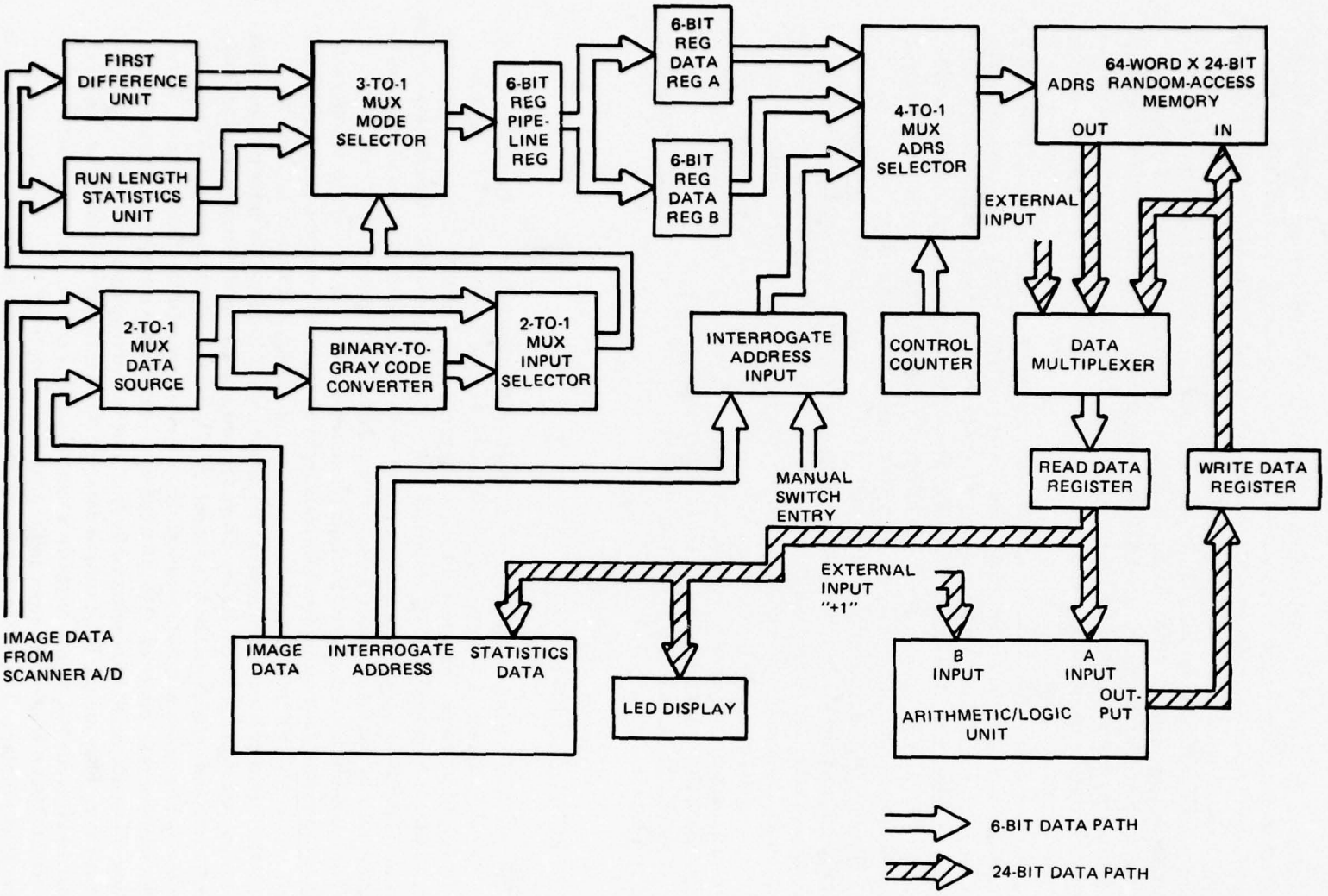


Figure A29. DIA block diagram.

ALU for writing into memory. The LED display provides manual readout of the contents of the RAM. The GPIB interface allows the MCU or the 4051 to read the contents of the RAM and display them in graphic or tabular form. The interface also allows the MCU to transfer image data from either the FSM or magnetic tape to the DIA.

The high-speed data interface is comprised of 10 ECL-compatible differential signals transmitted over twisted-pair lines. There are six data inputs, a clock, an enable, and a clear-memory signal with an echo output response after the memory is cleared. The maximum clock rate to the DIA is approximately 21 MHz. Currently the DIA is interfaced via this data input port to the USPS LDTB and to the VTS.

Incorporated in the DIA is a circuit which may be used to test its operation. A block diagram of the circuitry is shown in figure A30. It is driven by a voltage-controlled oscillator, with adjustable frequency, whose range is approximately 10 to 25 MHz. Also included is a programmable eight-position switch which may be used to select a desired binary count sequence for data generation. The variable clock rate allows testing of the analyzer at speeds up to 25 MHz.

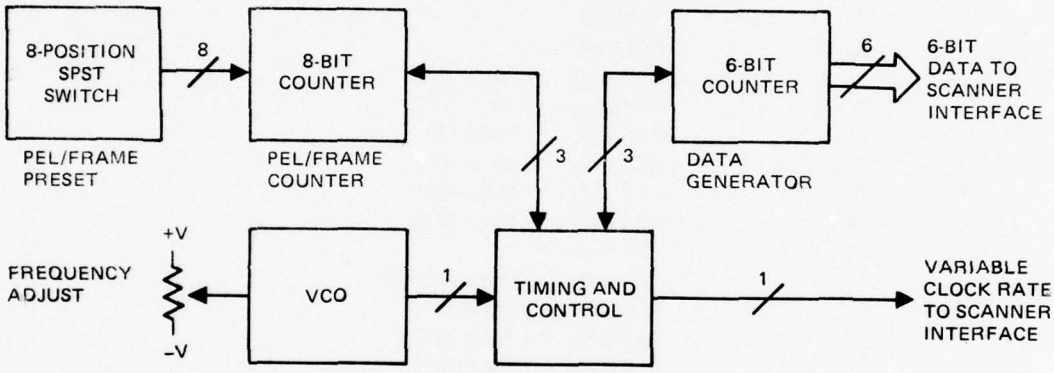


Figure A30. DIA built-in test equipment.

FRONT-PANEL CONTROLS

Figure A31 is a diagram of the DIA front-panel controls. On the left is a two-digit octal lever switch used for selection of any one of up to 64 operating modes. See table A3 for the modes implemented. The next two-digit octal lever switch selects any one of the 64 memory locations for manual readout of memory and for various diagnostic modes. The EXECUTE pushbutton is used to initiate the various diagnostic modes. The MASTER RESET pushbutton is used to clear various portions of the circuitry and to place the DIA under front-panel control. On the right is an eight-digit octal LED display used to read data from the memory. There is an additional mode which is designed to check the repeatability or the stability of an image sensor. Assuming that the pel brightness statistics were just accumulated, this new subtract mode may be run in a manner such that a memory location is decremented rather than incremented as in the previous mode. If the two images were identical, all memory locations should be decremented to exactly zero. In this way the differences in an image, from one scan to the next, will be shown by the resulting information left in the memory.

TABLE A3. DIA ANALYSIS MODES.

00	PBS Binary
01	RLS Binary 0-Runs BP-1 (LSB)
02	RLS Binary 0-Runs BP-2
03	RLS Binary 0-Runs BP-3
04	RLS Binary 0-Runs BP-4
05	RLS Binary 0-Runs BP-5
06	RLS Binary 0-Runs BP-6 (MSB)
07	FDS Binary
10	PBS Binary Subtract mode
11	RLS Binary 1-Runs BP-1
12	RLS Binary 1-Runs BP-2
13	RLS Binary 1-Runs BP-3
14	RLS Binary 1-Runs BP-4
15	RLS Binary 1-Runs BP-5
16	RLS Binary 1-Runs BP-6
17	Not used
20	PBS Gray
21	RLS Gray 0-Runs BP-1
22	RLS Gray 0-Runs BP-2
23	RLS Gray 0-Runs BP-3
24	RLS Gray 0-Runs BP-4
25	RLS Gray 0-Runs BP-5
26	RLS Gray 0-Runs BP-6
27	FDS Gray
30	PBS Gray Subtract mode
31	RLS Gray 1-Runs BP-1
32	RLS Gray 1-Runs BP-2
33	RLS Gray 1-Runs BP-3
34	RLS Gray 1-Runs BP-4
35	RLS Gray 1-Runs BP-5
36	RLS Gray 1-Runs BP-6
37	Not used
40	Display contents of selected register
41	Clear Memory
42	Store contents of "A" bus in selected register
43	Store contents of "A" bus in all registers
44	Continuous increment into selected register
45	Continuous decrement into selected register
46	
•	
•	Not used
•	
77	

Notes: PBS Pel Brightness Statistics
RLS Run Length Statistics
FDS First Difference Statistics

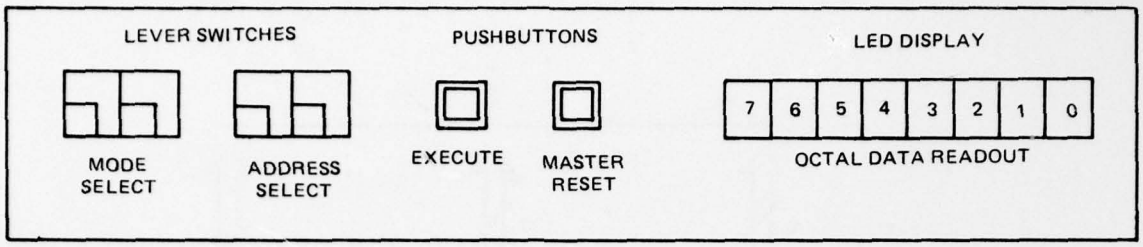


Figure A31. DIA front-panel controls.

GPIB INTERFACE DESCRIPTION

The GPIB interface allows the DIA to be used as a peripheral device under control of the Tektronix 4051 Graphic System, which is the GPIB controller. Under GPIB control, image data may be transferred to the DIA from the MCU for analysis and the results transferred back to the MCU for further processing and/or storage. The analysis data may also be transferred to the 4051 terminal for display.

Shown in figure A32 is a functional block diagram of the GPIB interface which is directly compatible with IEEE STD 488-1975. When the DIA is assigned as a listener on the GPIB, either mode control information or image data may be transmitted to the DIA from another device on the bus and stored in the mode control register or the image data register, respectively. When assigned as a talker on the GPIB, the DIA transmits the contents of the 64-word by 24-bit memory to the listening device(s) on the bus as a series of 192 eight-bit bytes (3 eight-bit bytes per 24-bit word).

One of the five interface control signals, REMOTE ENABLE (REN), is used to place the DIA under GPIB control. The DIA is returned to front-panel (local) control by pressing the RESET button on the front panel.

GRAPHICS TERMINAL

One of the major tasks assigned to the ICAS is to produce data on which design decisions may be based. Manual transcription of the volume of data being produced would be a virtually impossible task. Therefore, some form of human-readable display is necessary. In addition, the number of discrete operations to be performed by the system would be staggering were there no simplified man-machine interface. The obvious solution to both these problems with a single piece of equipment is an alphanumeric data terminal. The type of data produced lends itself to graphical interpretation in the form of histograms (bar-graphs) and curves, which is not easily accomplished on a simple alphanumeric terminal. For this reason, the Tektronix 4051 Graphic System has been incorporated into the ICAS.

The 4051 is a highly "intelligent" terminal allowing complete control of the ICAS as well as off-line data examination in both tabular and graphic formats. The 4051 may perform calculations on data which may be saved on an internal magnetic tape unit or received and transmitted on the IEEE GPIB. Commands to the ICAS may also be issued on the GPIB.

The 4051 operates either interactively or under program control, using an enhanced BASIC, implemented in 4051 firmware, which allows simplified invocation of the graphics features.

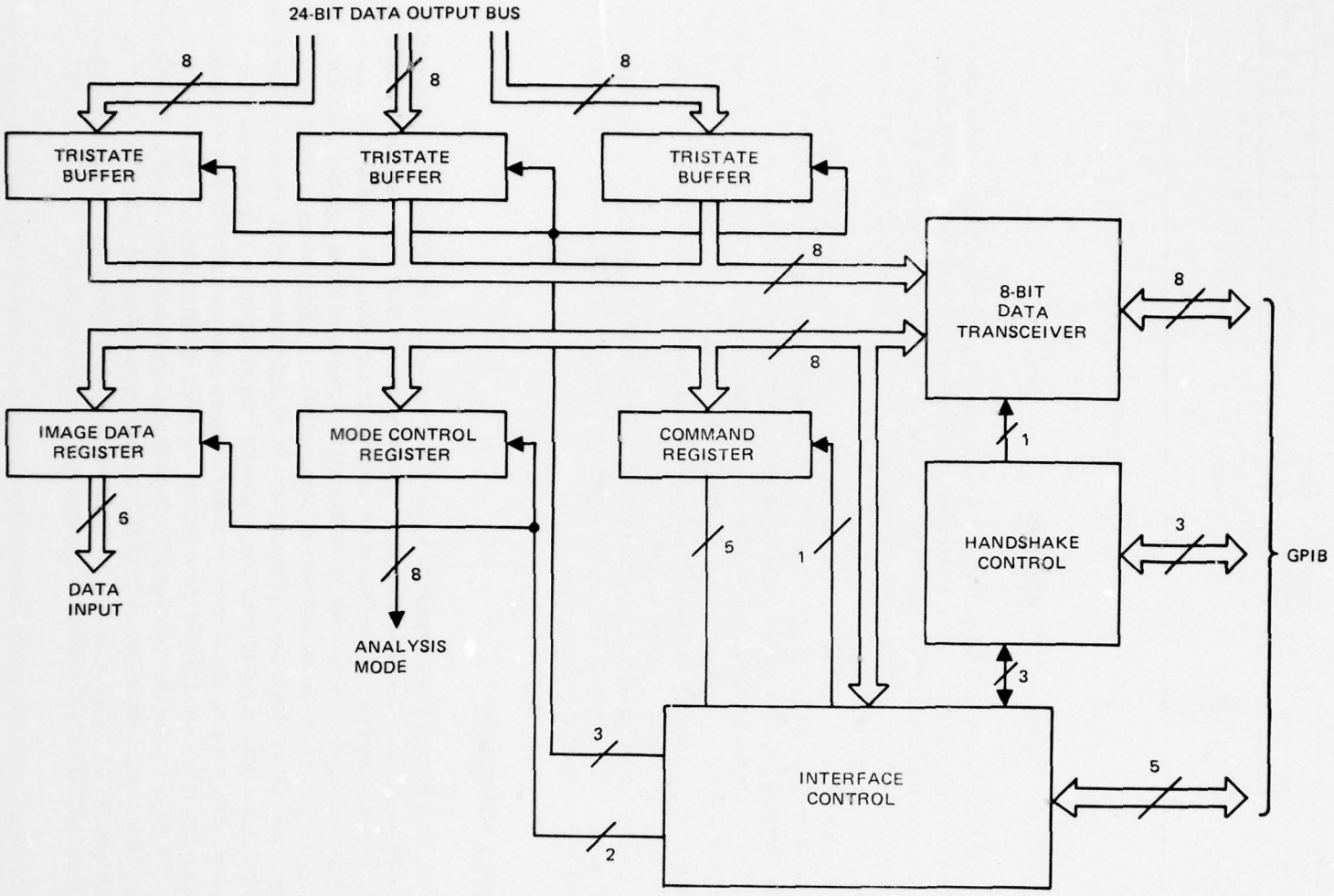


Figure A32. DIA general-purpose interface bus.

The primary features of the 4051 are as follows:

1. An LSI microprocessor computing module and an 8k-byte standard (expandable to 32k) workspace. All operations are invoked in high-level BASIC which includes built-in graphics and error detection.

2. Internal peripherals include: a full ASCII (128 character) keyboard with additional user-definable function keys and program editing keys; and a 300k-byte-capacity cartridge tape unit.

3. The CRT display (8 inches wide by 6 inches high) allows alphanumeric format, 35 lines of 72 characters each, and/or graphic display with a resolution of 780 (vertical) by 1024 (horizontal) points.

4. Completely asynchronous communication of ASCII or machine-dependent-binary code by use of the GPIB with three-wire handshake. The 4051 was designed as a GPIB controller and is capable of controlling all bus functions.

5. Interrupt service capability.

6. Physical characteristics are: 34.5 cm high, 46.5 cm wide, and 82.6 cm long; and 29.5 kg (weight).

PRINTER/PLOTTER

In addition to viewing data interactively, ie, as produced, it is highly advantageous to have the capability to refer back to data at some later point in time. For this capability, some form of hard copy is needed. Manual transcription can be ignored because of the large volume of data produced. Therefore, an electronically controllable hard-copy device is necessary.

There are two basic types of hard-copy devices available – impact and nonimpact. Impact hard-copy units (printers) are fully mechanical. In addition, printers are restricted to character printing and allow only encoded character data as input. Nonimpact printers use a variety of techniques including ink jet, laser, and electrostatic.

There are several advantages of nonimpact over impact printers. These include decreased noise, wear, and misalignment, and, in the moderate price range, higher resolution. In addition, nonimpact devices are capable of accepting point input rather than being restricted to character input. This feature is of particular advantage when a graphic hard copy is required.

The electrostatic process was chosen as the ICAS hard-copy method because of its relatively low cost. The Versatec 1200A, specifically, was chosen for three reasons: (1) it offers a plot resolution of 200 by 200 points per inch; (2) it can either print, plot, or print and plot simultaneously; (3) it is plug-compatible with the Tektronix 4051 Graphic System. The 200-by-200 resolution allows the ICAS to print thresholded (1 bit) USPS images at the required resolution. The print and plot capability allows the memory control unit to output to the 1200A textual information, data from analysis or other calculations, thresholded images, or all three simultaneously, if desired. The plug-compatibility with the 4051 allowed the 1200A to be immediately incorporated into the ICAS for data plotting (from the CRT) before the MCU interface for the 1200A was completed.

The 1200A, which includes a character generator, features a 16-by-16 dot-matrix roman type font. Paper is available in both roll and fanfold types, allowing for greater compatibility with USPS printing requirements. Paper drive is incremental, simplifying MCU interface requirements. The parallel data rate is 1 million characters or 8 million plot (image) points per second. Physically, the 1200A is 19 inches wide, 18 inches deep, and 38 inches high.

MAGNETIC TAPE SUBSYSTEM

The video frame-storage memory in the ICAS is volatile, which means that all data and image information is lost when power is removed. In order to maintain permanent records, save results for later use, save programs, etc, it is necessary to resort to relatively slow but nonvolatile magnetic storage. This requirement is satisfied with a commercial nine-track magnetic tape system consisting of a Format Control Unit (FCU) and two synchronous, 2400-foot-reel tape drives (the FCU can control up to four tape drives).

The tape subsystem performs two important functions within the ICAS. First, captured images, processed images, tables, and other image-related data are maintained in a tape library as a permanent record of experimental results. Second, all system programs are stored on tape and can be loaded into program memory with a ROM bootstrap.

As discussed in previous sections, the magnitude of the image to be captured and stored is nearly 23 million bits, or about 3 million bytes. Magnetic tape is the only nonvolatile storage medium combining high-reliability, proved technology with large storage capacity, and reasonable cost-speed tradeoff. However, even using the highest possible storage density in moderate-cost tape equipment, only about nine images can be recorded on a single 2400-foot tape. Specific parameters of the tape equipment are as follows:

Speed	45 ips
Format	"IBM compatible"
Density	Dual 800/1600 cpi
Width	1/2-inch tape
Tracks	9 (8 data, 1 parity)
Error checking	VRCC, LRCC, CRCC

An additional justification for choosing magnetic tape for image storage is that it is virtually the universal medium for the transmittal of processed images. The most common format for image records is as follows:

1 image	= one file (separated from other files by a "filemark")
1 video line	= one record (separated from other records by an "interrecord gap")
1 video pel	= one character (1 byte = 8 bits)
Record density	= 800 cpi

Although this format is conceptually simple, it does not achieve the most efficient use of tape. Two formats have been implemented in the ICAS. The quasi "industry standard" image tape format described above has been used at NOSC in order to maintain compatibility with other agencies in image acquisition and processing. This format is only efficient, however, when the video information is digitized to 8 bits or 256 grey levels. Since the ICAS is only required to convert video to a 6-bit sample, 2 bits out of each tape character are not used. Therefore, one-fourth of the tape storage capacity is wasted. For in-house use, therefore, one and one-third pels are packed into each tape character, achieving higher storage efficiency and higher data transfer rates. Also, the data are stored at 1600 cpi, which represents an additional 2-to-1 increase in storage efficiency and speed parameters.

The amount of tape required to store a video line in the best format described above can be calculated from

$$\text{tape length/line} = \frac{\text{pels/line}}{(\text{pels/char})\,(\text{char/inch})}\ (\text{eg}) = \frac{1728}{(4/3)\,(1600)} = 0.81 \text{ inch}$$

which shows that 0.8 inch of tape is used for each video line. Since the interrecord gap is nominally 0.6 inch, the total tape length used for a USPS image is

(2200 lines) (1.41 in/line) = 3102 in/image = 258.5 ft/image.

An additional improvement of nearly 20% in density and speed could be achieved by packing two video lines into one tape record.

$$(1100)\,(06 + .81 + .81) = (1100)\,(2.22) = 2422 \text{ in/image}$$
$$= 203.5 \text{ ft/image.}$$

IEEE STD 488 COMMUNICATIONS INTERFACE (GPIB)

INTRODUCTION

The GPIB is a standard interface originally designed (and patented by Hewlett-Packard) to interface programmable instrumentation systems with a digital computer in such a way as to satisfy the most frequent needs of such systems. The following are the basic criteria of the standard: to support data rates up to 1 megabyte per second; to support distances up to 20 metres; to support up to 15 devices running simultaneously; and to optimize communication methods for devices with typical message lengths of 10–20 characters. General attributes of the GPIB are: asynchronous communication using a three-wire handshake; direct communication between devices without requiring all messages to be routed through a control unit; design elegance; and device-independence of the major interface sections.

There are four elements to an interface system: mechanical (connectors and cables); electrical (voltage and current values); functional (signals, protocol, timing, interface functions); operational (device-independent responses to interface signals). The GPIB makes all but the operational elements device-independent, thereby allowing any device to use the bus by implementing only those functions required by the device. Because some devices perform output only ("talkers") and some perform input only ("listeners"), the individual interfaces may delete "listener" and "talker" functions, respectively.

FUNCTIONAL SPECIFICATIONS

There are 10 interface functions, each with one or more allowable subsets. The only requirement for an individual interface is that it be able to handshake on data and recognize its own address. The standard bus consists of 16 signal lines organized as three sub-buses: an 8-bit data bus, a 3-bit transfer or handshake bus, and a 5-bit management bus. The minimum configuration includes the data bus, the transfer bus, and the ATN signal, which is the bus controller's management line. Figure A33 shows the general case of the GPIB structure and capabilities. The following is a brief statement (including IEEE document section) of each of the interface functions implemented and of the MCU and 4051 conformance to the standard.

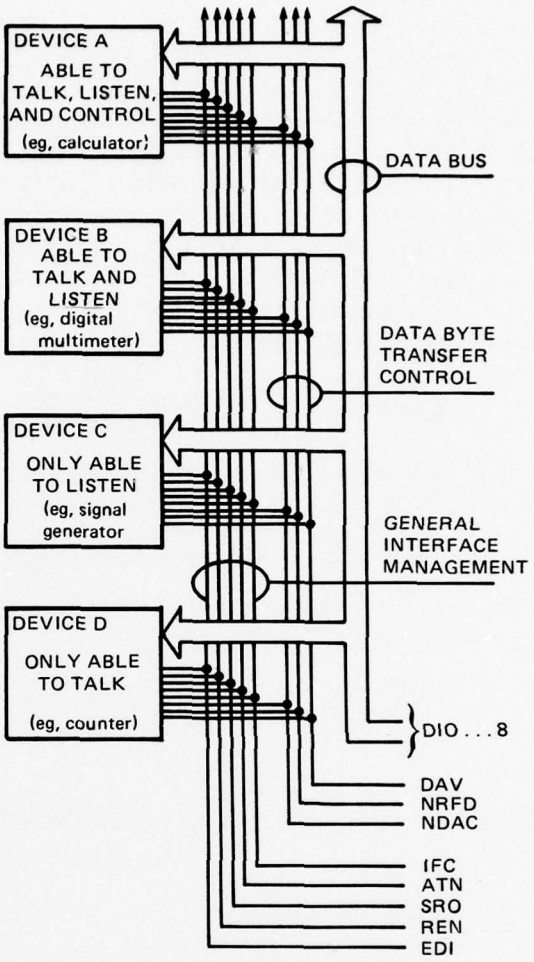


Figure A33. GPIB interface capabilities and bus structure.

1. The SH (Source Handshake, section 2.3) function allows a device to initiate and terminate data transfers on the data bus. Both the 4051 and the MCU are capable of transmitting asynchronous messages on the bus.

2. The AH (Acceptor Handshake, section 2.4) function allows a device to receive asynchronous messages on the bus. Asynchronous communication is guaranteed by an interlocked handshake between one SH function and one or more AH functions. Both the 4051 and the MCU can receive asynchronous messages on the bus.

3. The T (Talker, section 2.5) function (and its extension TE) allows a device to send device-dependent data to other devices when the function is addressed to talk. The T function is addressed with a single byte, TE with 2 bytes. The 4051 honors secondary addresses (or commands) but prohibits other devices from polling the status of the 4051 since it is the system controller. The MCU T function is identical except that its interface status may be polled by other devices on the bus.

4. The L (Listener, section 2.6) function allows a device to receive device-dependent data when the function is addressed to listen. The LE function allows 2-byte addressing. The 4051 honors secondary addresses and allows the 4051 to remove itself from the bus as a listener. The MCU can be both a talker and a listener.

5. The SR (Service Request, section 2.7) function allows a device to asynchronously request service from the controller in charge of the interface. Because the 4051 is the interface controller, it has no need to issue service requests but is capable of honoring them. The MCU has service request capability.

BUS OPERATION

The GPIB is composed of three buses – the data bus, the management bus, and the transfer bus:

1. Data Bus. The data bus is an 8-bit (1 byte) bus on which are transferred peripheral addresses (primary and secondary), control words, and data bytes. Data bytes may be either ASCII or machine-dependent binary code.

2. Management Bus. The management bus consists of five signal lines which control data transfers over the data bus. The management bus signals are as follows:

   a. Attention (ATN) is activated by the controller when peripheral devices are being assigned as talkers and listeners. Only peripheral addresses and control messages can be transferred over the data bus when ATN is active. After ATN becomes inactive, only those devices designated as talkers or listeners may take part in the data transfer. The use of ATN is strictly controlled by user programs in the 4051.

   b. Service Request (SRQ) may be set by any device on the GPIB which desires the attention of the controller, which in turn sets ATN and executes a serial poll to determine which device is requesting service.

   c. Interface Clear (IFC) is activated by the controller in order to place all interface circuitry in a known quiescent state.

   d. Remote Enable (REN) is activated whenever the system is operating under program control and causes all devices to ignore their own front-panel controls.

   e. End Or Identify (EOI) is used by the talker to indicate the end of a data transfer sequence and is activated as the last byte of a message is transmitted. When the controller is listening, it assumes that a data byte received is the last byte in the transmission if EOI is activated. When the controller is talking, it always activates EOI as the last byte is transferred.

3. Transfer Bus. A handshake sequence is executed by the talker and listeners over the transfer bus each time a byte is transferred over the data bus. The transfer bus signals are:

   a. Not Ready For Data (NRFD), which indicates that one or more listeners are not ready to receive the next data byte.

   b. Data Valid (DAV), which is activated by the talker shortly after placing a valid data byte on the data bus. DAV cannot be activated when NRFD is active.

c. Data Not Accepted (NDAC), which is active until each listener has captured the data byte currently being transmitted.

Software control of the GPIB is provided for in the 4051 extended BASIC language and is implemented in 4051 firmware. The primary BASIC I/O commands are PRINT and INPUT. In standard BASIC these commands imply certain devices. By default, in the 4051, they refer to the display and keyboard, respectively. By adding addresses to the statement, any device on the bus may be accessed with the same commands.

The control lines such as ATN, DAV, NRFD, and NDAC are handled automatically by the PRINT and INPUT keywords. The bus commands UNTalk and UNListen are issued automatically at the end of these I/O operations, in order to shut down the bus.

Each device on the GPIB is given a device number called a primary address. Specifying a primary address in a BASIC statement selects a device for an I/O operation. For example, for the print (output) operation, PRINT @ 33: specifies the internal magnetic tape unit and PRINT @16: specifies peripheral device number 16 as the output device.

Associated with each primary address may be one or more secondary addresses which impart information to the selected device concerning the data format or a subdevice address. For example, the default secondary address for the PRINT statement is 12, specifying an ASCII data string transfer.

Binary commands such as WBYTE and RBYTE allow the output or input, respectively, of any 8-bit binary pattern. This allows the selective addressing of multiple listeners on the GPIB and complete control of the GPIB control lines.

The 4051 is capable of honoring interrupts by any device pulling the SRQ line to active low, whenever interrupt is enabled. Interrupts may occur either during program execution or while the 4051 remains idle. When the SRQ is activated, the interrupting device is located by the execution of a software serial POLL of all devices capable of generating an SRQ. When the device is located, program control is transferred to the service routine for the interrupting device.

The POLL statement syntax is:

POLL A,B: DV1;DV2; ...;DVn

A and B are simple numeric variables. A is the device identifier and B is the device status. DV1 through DVn are device numbers to be polled. After DVi is identified as the interrupting device, the value i is assigned to variable A and an 8-bit status byte presented by the device specified by CVi is assigned to variable B. These variables allow easier execution of the desired interrupt service routine.

HARDWARE IMPLEMENTATION

The GPIB is implemented in MCU hardware essentially as a group of state counters, with transitions between states clearly defined by the 488 standard. Figures A34 through A38 show the state diagrams of the subset of the standard implemented in the MCU. Referring to figures A35 and A37, the following is an example of a typical single-byte transfer from the 4051 to the MCU from the viewpoint of the MCU interface. The 4051 BASIC command WBYTE@ 33,108:-65 transmits the ASCII representation of the letter A or the number 65 (the data are identical; the interpretation is the responsibility of the MCU) to the MCU.

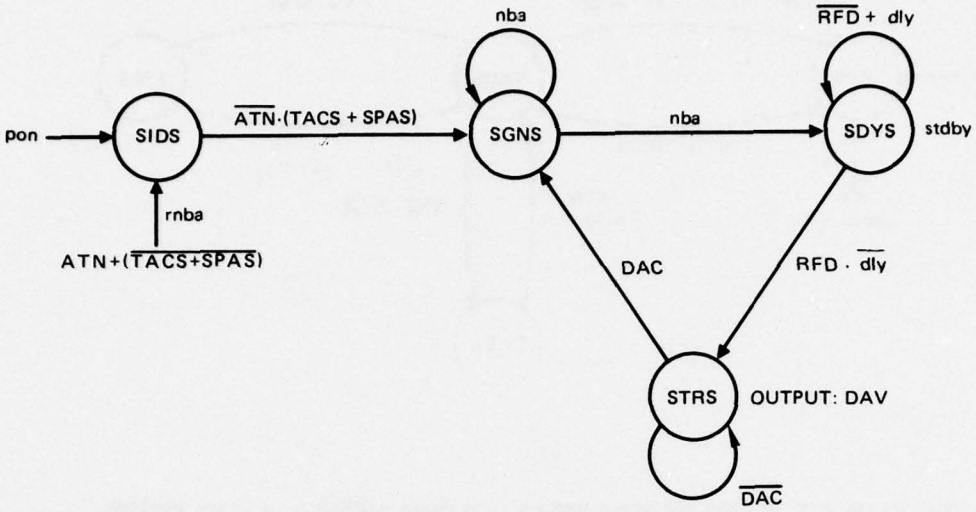


Figure A34. GPIB Source Handshake state diagram.

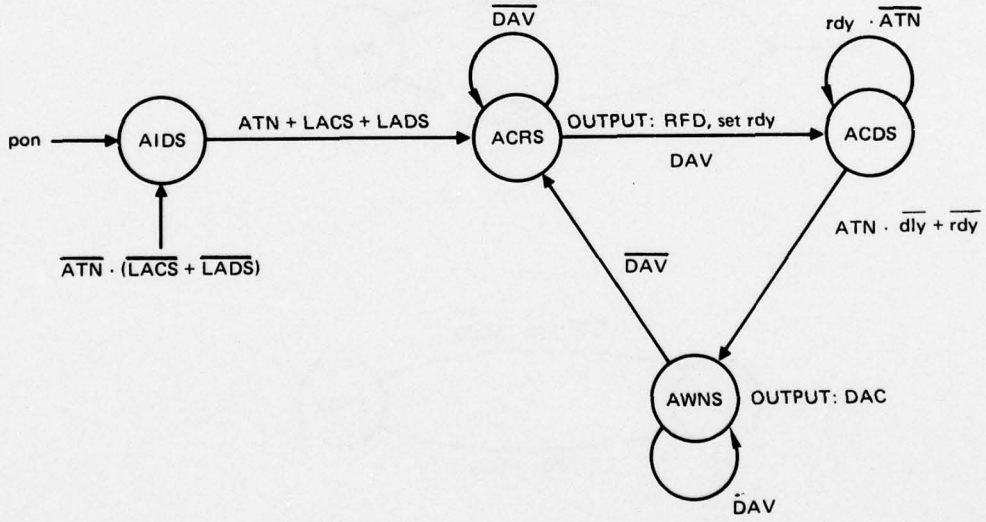
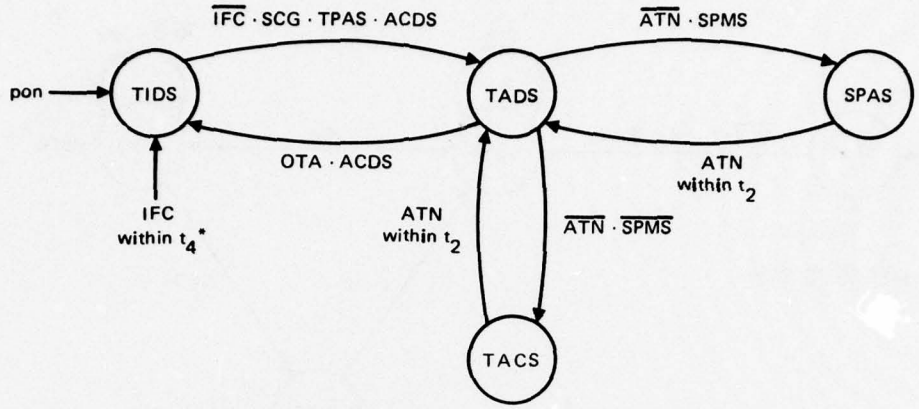
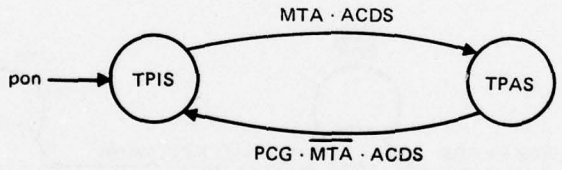


Figure A35. GPIB Acceptor Handshake state diagram.



*t_2 and t_4 are maximum time intervals for occurrence of these signals as defined by IEEE std 488-1965.



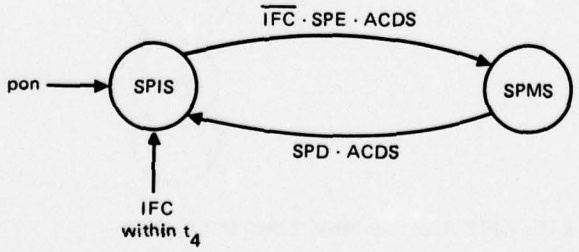


Figure A36. GPIB Talker Extended state diagram.

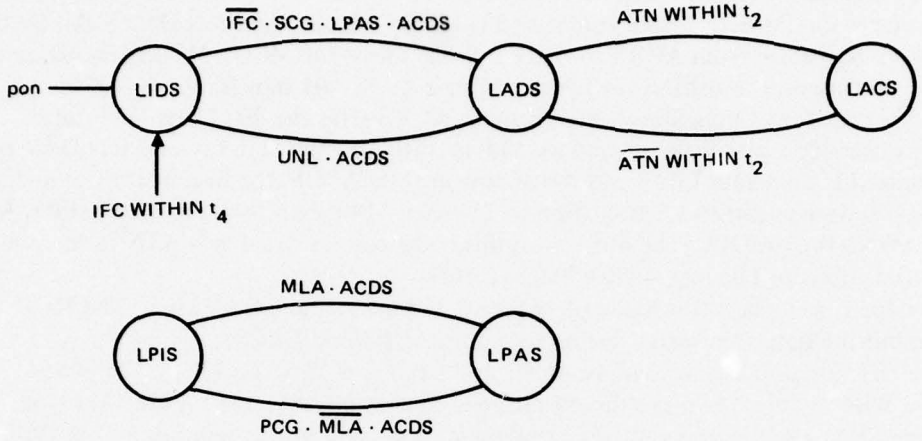


Figure A37. GPIB Listener Extended state diagram.

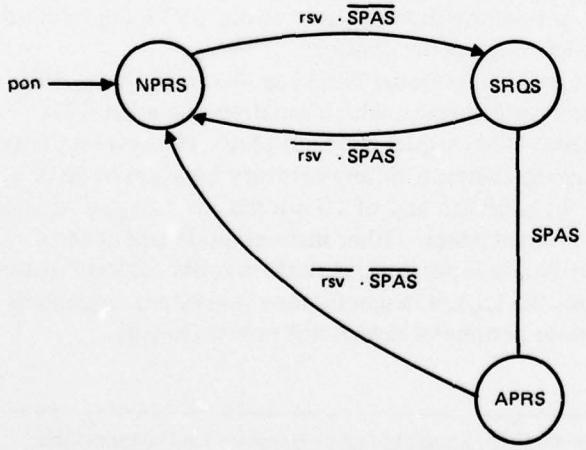


Figure A38. GPIB Service Request state diagram.

Assume a power-on (pon) has just occurred, which places the AH function in state AIDS (Acceptor Idle State) and the LE function in states LIDS (Listener Idle State) and LPIS (Listener Primary Idle State). The 4051 encounters the command WBYTE@ 33,108: -65 which causes ATN to become active.

With ATN active, AH transitions from AIDS to ACRS (ACceptor Ready State). The 4051 then places the Primary Listen Address (33) on the data bus and sets Data Valid (DAV), which causes a transition from ACRS to ACDS. Since this is the MCU's My Listen Address (MLA), the LE function transitions to LPAS. After a delay, AH transitions to AWNS (Acceptor Wait for New Cycle State), then back to ACRS after the 4051 sets DAV false.

Next, the 4051 places the secondary address (108) on the data bus and sets DAV true again. Because LE is in state LPAS and AH is now in state ACDS, the Secondary Command Group (SCG) code 108 causes LE transition to Listener ADdressed State, and, as before, AH returns to AWNS then ACRS. The 4051 encounters the colon (:) and sets ATN false upon which LE transitions to Listener ACtive State (LACS).

The 4051 now places the value 65 on the data bus, and sets DAV true. The MCU may now input the data value after testing for states ACDS and LACS.

The AH function is now in state ACRS and LE is in LACS and LPAS. The 4051 must issue a WBYTE@63: to place these functions back in an idle state. ATN is set true, which places LE in LADS. The value 63 (UNListen) is placed on the data bus and DAV is set true, placing AH in ACDS, which in turn sets LE back to LIDS and LPIS. ATN is then set false, which in turn sets AH to state AIDS.

For a more detailed description as well as further examples of GPIB operation, the reader is directed to references A3 and A4.

MEMORY CONTROL UNIT

The memory control and support hardware constructed at NOSC performs two principal functions: display of a stored image on a cathode ray tube (raster-type display) and processing or analysis of the digital video image data as appropriate. The Memory Control Unit (MCU) has been constructed from off-the-shelf, state-of-the-art, TTL digital hardware and based on the Intel 3000 series LSI computing devices.

The hardware is composed of six major functional blocks as shown in figure A39. The video output logic contains the output multiplexer, which serializes the eight 6-bit video samples in a 48-bit word into a digital video sequence for display. The system contains a manual control panel which can display the contents of any memory location or store a 48-bit word into any memory location. In addition, any of 10 internal scratch pad registers may be displayed or modified from the control panel. Other manual mode and control functions are also provided. A set of peripheral input/output ports permits communications between the memory, the control system, the DIA, a magnetic tape subsystem, a graphics display terminal, and any other appropriate peripheral device not now included.

A3 Institute of Electrical and Electronics Engineers, IEEE Standard Digital Interface for Programmable Instrumentation, IEEE STD 488-1975, ANSI MC1.1-1975, April 4, 1975

A4 Laroff, Gary P, Tektronix GPIB Applications Support, Tektronix, Inc, Boston, 1976

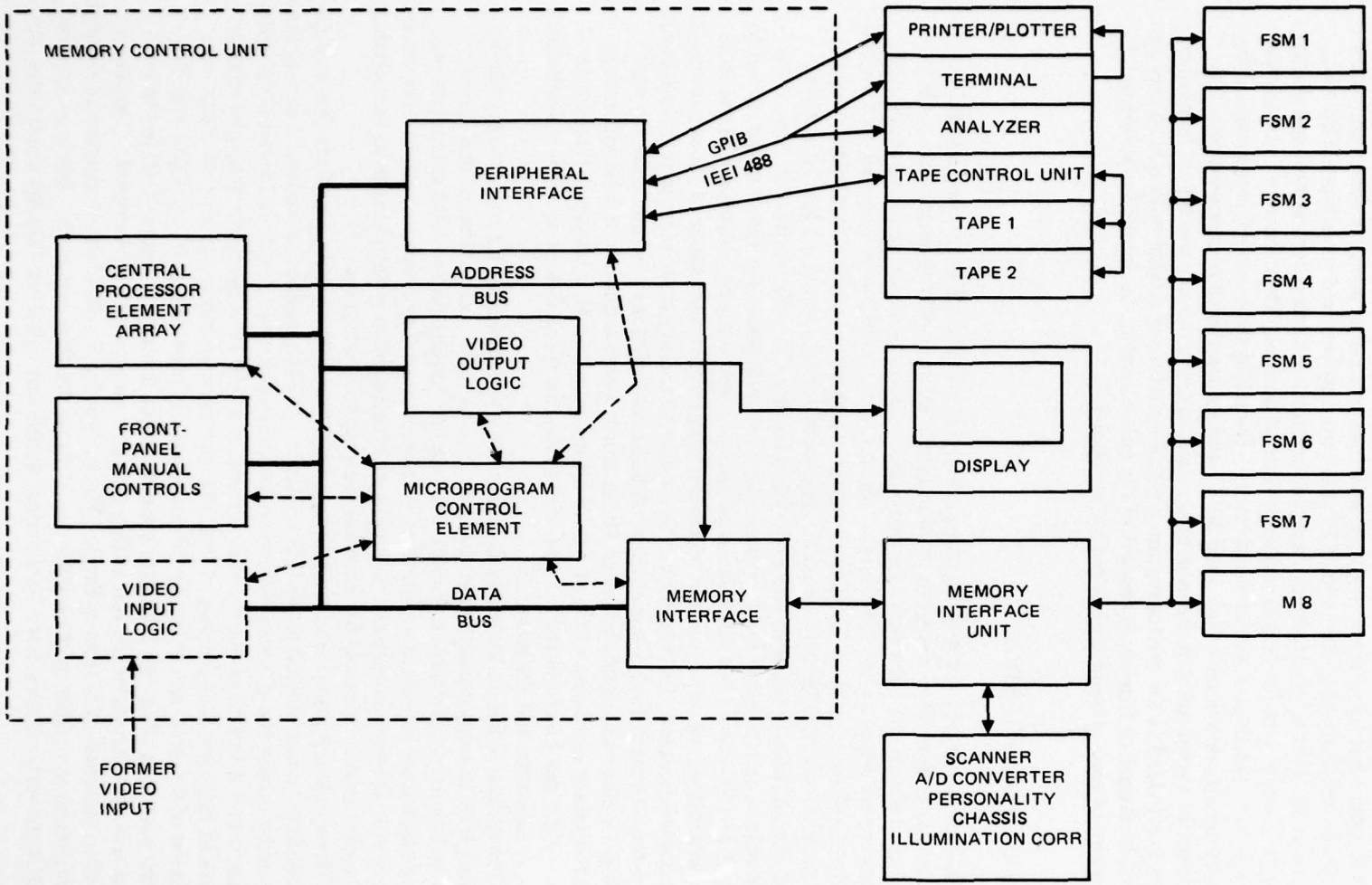


Figure A39. MCU block diagram.

The upper left hand block in figure A39 (the processing array) is composed of 24 Intel 3002 central processing elements (CPEs), commonly referred to as bipolar bit slices. These devices are used to generate and maintain memory addresses for capture and display as well as to process data for transferral to peripheral devices. They therefore provide the ability to process video data within the memory. Overall system control is maintained by the microprogram control unit (one Intel 3001) and its associated micromemories. All control functions performed in the system are derived from this control logic. Extensive versatility is provided in the microprogram control structure to enable both macrolevel and microlevel (software or firmware) control of the entire system. A detailed description of the operation of each subunit within the MCU follows.

VIDEO OUTPUT LOGIC

In order to display a captured image, the FSM and the MCU are used as a refresh memory and sync generator, respectively, for a raster-scan display monitor. Each 48-bit memory word represents eight pels of a video line. Address generation for memory read operations is performed by the CPE array. Since the captured image is stored on a sequential line-by-line basis, and the CRT display monitor generates an interlaced raster, some address calculations must be performed at the conclusion of each video line to achieve interlace. In addition to video refresh generation for the CRT, the control section of the system generates independent horizontal and vertical sync pulses for the monitor, timed to achieve a 2 to-1 interlace. Standard line sync rates are not required, since the Conrac RQB monitor will phase-lock and maintain synchronization over a wide range of input horizontal and vertical frequencies. The system has the ability to modify these rates in real time during vertical retrace to alter display parameters. Additional functions performed by the video output logic include the multiplexing of 48-bit words into a sequence of 6-bit video pels having a frequency eight times that of the 48-bit memory words. Subsequent logic is included to select any precision from 1 to 6 bits or any bit plane from 1 to 6 for presentation to the D/A converter and the monitor.

The output video multiplexing is performed by reading a 48-bit word from memory and storing it in an output register via the data bus. A 3-bit binary counter and 3-to-8 decoder is then used to selectively enable 6-bit tristate buffers onto a 6-bit video data bus. The same clock used to increment the binary counter is used to clock successive 6-bit video samples to a 6-bit retiming register. The pel-serial digital video is then sent to an arrangement of data selectors (multiplexers) for bit plane/bit precision selection.

The bit plane/bit precision logic must either select one of the six bit planes or one of six bit precisions to be transmitted to the D/A converter. It is important that no loss of analog dynamic range occur during the process. As shown in figure A40, the 6-bit digital video is presented to a single 8-to-1 bit-plane-select multiplexer and to a 2-to-1 bit precision multiplexer stage. Operation of this logic is as follows. First, a bit precision is selected from 1 of 6 bits. If a bit precision of 0 is selected, then the output of the bit plane selector is enabled into all output bit positions. Copying logic (for simplicity not detailed in figure A40) in the bit precision selectors maintains the full analog dynamic range in the D/A output. Consider a bit precision selection of 5 as an example. The high-order 5 video bits are connected through line driver/receiver circuits to the high-order 5 bits of the D/A converter. The low-order bit of the D/A converter is connected to the most significant video bit, thereby duplicating the

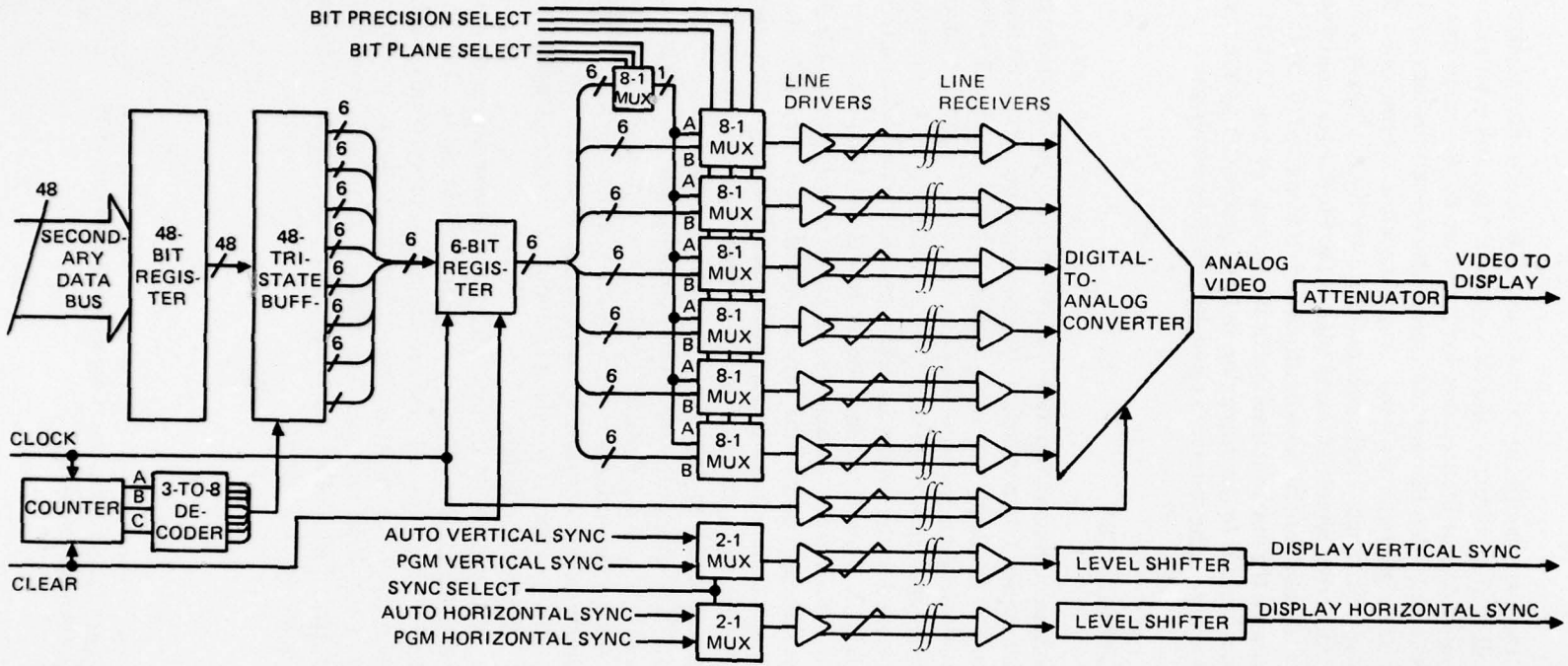


Figure A40. Video output and unpacking logic.

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ADVANCED MAIL SYSTEMS SCANNER TECHNOLOGY. EXECUTIVE SUMMARY AND--ETC(U)
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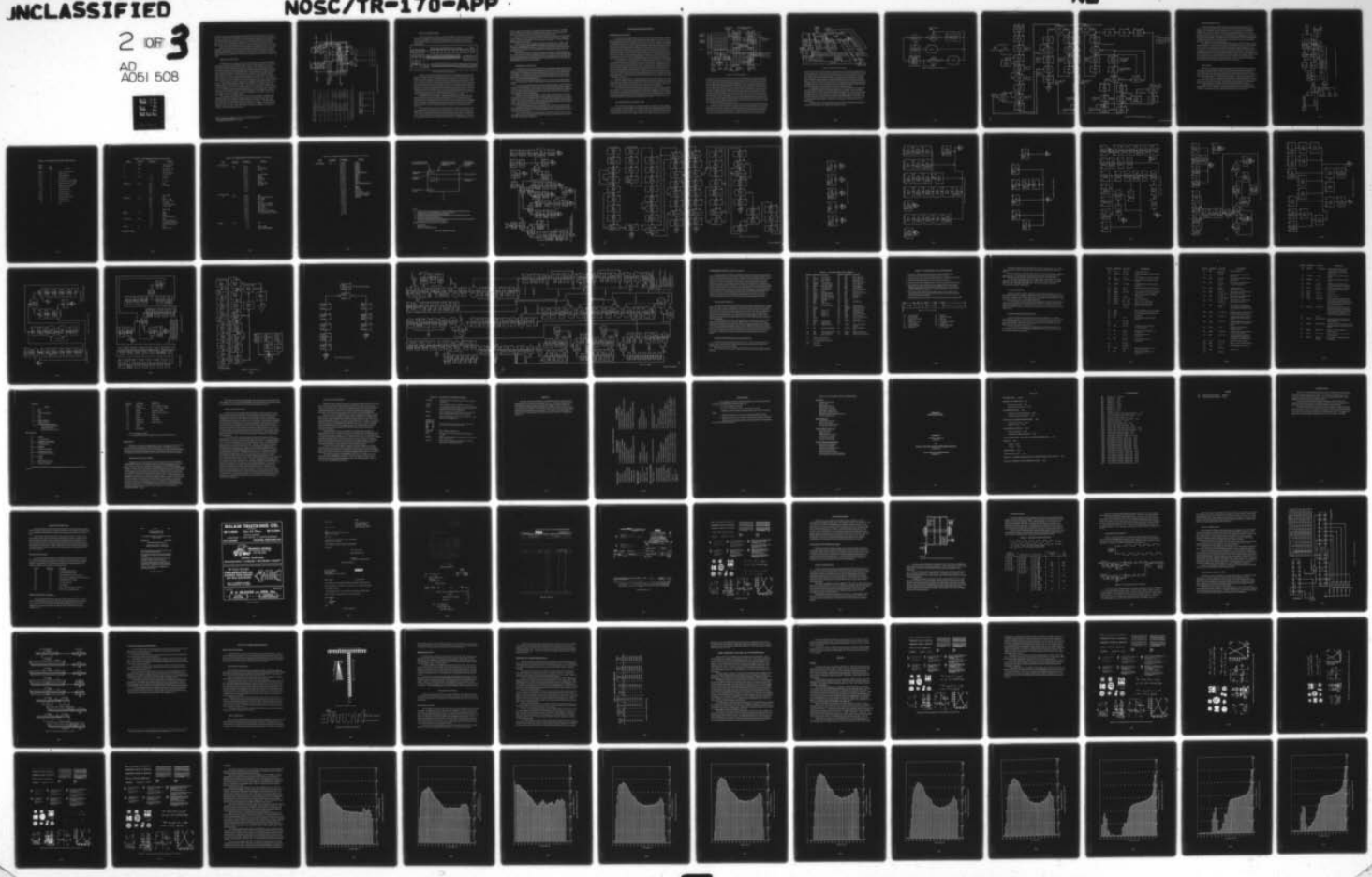


most significant bit in the least significant bit position. This connection assures that a video sample of value 00_8 will be transmitted to the D/A converter as a full 6-bit zero value and 77_8 as the maximum value. Lower bit precision selections are implemented in a similar fashion such that the highest selected video bits are connected directly and the unused low-order positions are copies of the high-order positions. Any connection scheme other than this either sacrifices D/A dynamic range or produces excessive nonlinear steps in the video output.

Since the D/A converter (which is located adjacent to the display) contains its own retiming register, the same clock used for the video multiplexer is transmitted to the D/A converter. Additional timing signals are the horizontal and vertical sync pulses for the display. Either the program-generated syncs are sent to the display or, in their absence, automatic sync signals are substituted in order to maintain the monitor's phase-locked loops within their normal operating range.

PROCESSING CIRCUITRY

The MCU generates command functions for the memory and monitors status replies in order to perform the required data transfers. Since the capture operation is a line-by-line, noninterlaced function and the display monitor requires a 2-to-1 interlaced video input, some form of address calculation is required. For example, if the incoming video data are stored sequentially during the capture operation, then, for display of that image, every other video line must be presented to the display as field 1 and the second set of alternating lines must be displayed as field 2. This means that the controller must sequentially output the video on line 1 of field 1, then add a constant (equal to the number of words per line) in order to skip the next line, and output the second line of the same field. In addition to address calculation, direct arithmetic or logical manipulation of the video image is desirable.

The processing circuitry is comprised of a standard register arithmetic logic unit (RALU). The hardware selected to implement the RALU is the Intel (second-sourced by Signetics) 3002 Central Processing Element. The 3002 chip is a Schottky bipolar LSI circuit containing a 2-bit slice of a complete RALU. It is expandable in 2-bit increments by use of additional chips, and optional lookahead carry, to any desired word width. The chip contains an arithmetic logic unit (ALU) recognizing 39 basic arithmetic and logical commands. A total of 13 registers is provided including an accumulator, a memory address register, and 11 scratchpad registers.

The complete MCU utilizes 24 of the 3002 chips to assemble a complete 48-bit processing section plus three fast lookahead carry (Intel 3003) chips. The 48-bit-wide RALU provides all the flexibility for address generation, memory control, and video processing that is now required or might be required in the future. A detailed description of the operation of the 3002 and associated devices is available from both Intel and Signetics (ref A5 and A6). Figure A41 shows the 3002 block diagram and summarizes the basic operations implemented therein.

A5 Series 3000 Reference Manual, 98-221A, Intel Corporation, Santa Clara, 1975

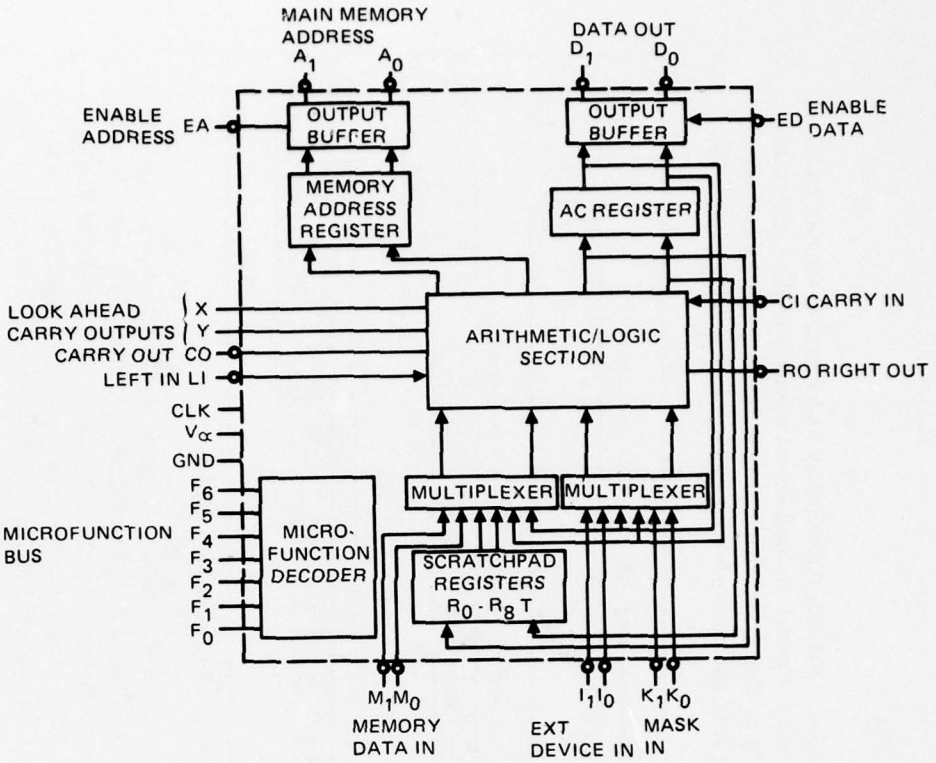
A6 Introducing the 3000, Signetics, Sunnyvale

F-GROUP	R-GROUP	MICROFUNCTION	
0	I	$R_n + (AC \wedge K) + CI \rightarrow R_n$ AC	
	II	$M + (AC \wedge K) + CI \rightarrow AT$	
	III	$AT_L \wedge (\overline{I_L \wedge K_L}) \rightarrow RO$	$LI \vee (I_H \wedge K_H) \wedge AT_H \rightarrow AT_H$ $\lvert AT_L \wedge (I_L \wedge K_L) \rvert \lvert AT_H \vee (I_H \wedge K_H) \rvert \rightarrow AT_L$
1	I	$K \vee R_n \rightarrow MAR$	$R_n + K + CI \rightarrow R_n$
	II	$K \vee M \rightarrow MAR$	$M + K + CI \rightarrow AT$
	III	$(\overline{AT} \vee K) + (AT \wedge K) + CI \rightarrow AT$	
2	I	$(AC \wedge K) - 1 + CI \rightarrow R_n$	(SEE NOTE 1)
	II	$(AC \wedge K) - 1 + CI \rightarrow AT$	
	III	$(I \wedge K) - 1 + CI \rightarrow AT$	
3	I	$R_n + (AC \wedge K) + CI \rightarrow R_n$	
	II	$M + (AC \wedge K) + CI \rightarrow AT$	
	III	$AT + (I \wedge K) + CI \rightarrow AT$	
4	I	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$	$R_n \wedge (AC \wedge K) \rightarrow R_n$
	II	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$	$M \wedge (AC \wedge K) \rightarrow AT$
	III	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$	$AT \wedge (I \wedge K) \rightarrow AT$
5	I	$CI \vee (R_n \wedge K) \rightarrow CO$	$K \wedge R_n \rightarrow R_n$
	II	$CI \vee (M \wedge K) \rightarrow CO$	$K \wedge M \rightarrow AT$
	III	$CI \vee (AT \wedge K) \rightarrow CO$	$K \wedge AT \rightarrow AT$
6	I	$CI \vee (AC \wedge K) \rightarrow CO$	$R_n \vee (AC \wedge K) \rightarrow R_n$
	II	$CI \vee (AC \wedge K) \rightarrow CO$	$M \vee (AC \wedge K) \rightarrow AT$
	III	$CI \vee (I \vee K) \rightarrow CO$	$AT \vee (I \wedge K) \rightarrow AT$
7	I	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$	$R_n \bar{\oplus} (AC \wedge K) \rightarrow R_n$
	II	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$	$M \bar{\oplus} (AC \wedge K) \rightarrow AT$
	III	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$	$AT \bar{\oplus} (I \wedge K) \rightarrow AT$

NOTES:

1. 2's complement arithmetic adds 111. . . 11 to perform subtraction of 000 . . . 01.
2. R_n includes T and AC as source and destination registers in R-group 1 microfunctions.
3. Standard arithmetic carry output values are generated in F-group 0, 1, 2, and 3 instructions.

FUNCTION GROUP	MICROFUNCTION INPUT F_6	5	4
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1



REGISTER GROUP	REGISTER	MICROFUNCTION INPUT F_3	2	1	0
I	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1	0
	AC	1	1	1	1

Figure A41. 3003 block diagram and instruction set.

MANUAL CONTROL PANEL

In order to operate the system, a manual data display and function control panel is provided. It is possible, from the control panel, to load 48-bit words into the accumulator or any register, display the contents of the accumulator or any register, and control the clock and mode functions. Figure A42 shows the layout of the various switches and displays available.

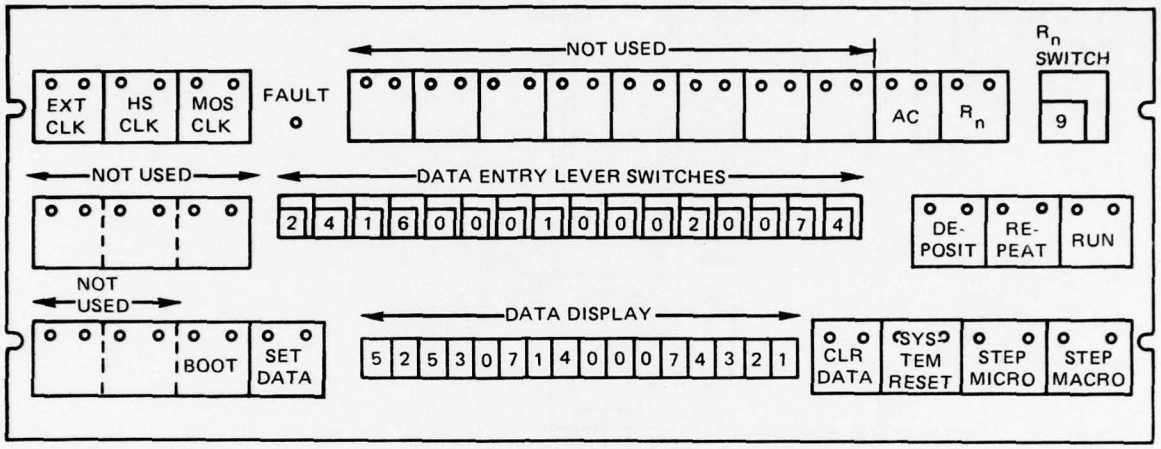


Figure A42. MCU manual control panel.

Sixteen octal-coded lever switches are provided to enter 48-bit data words into the system. Solid-state buttons and an additional decade lever switch permit data entry to any register or to the accumulator. These registers may be examined on 16 octal-coded displays located directly below the lever switches. Operation of the manual data transfers is as follows. A register is selected by touching the accumulator (AC) button or the R_n button with R_0 - R_9 selected on the R_n switch. Each time the AC or R_n button is touched, the display presents the contents of the selected register. Data entry is accomplished by setting the desired value into the switch register (lever switches) and touching the SET button. The data on the lever switches will be transferred to the selected register and then will be displayed. A CLEAR button is also provided. Operation is like that of the SET button except that the lever switches are ignored and the value of the selected register is set to zero.

A DEPOSIT button is provided to enable the manual entry of 48-bit words into a selected main memory location. This is accomplished by the following procedure. First, register R_7 is selected and the desired memory location is set into the low-order 16 bits. The data word to be loaded into memory is then set on the lever switches and the DEPOSIT button is touched. This operation transfers data from the lever switches to the memory location specified by R_7 and subsequently displays the contents of the memory location ($R_7 + 1$).

Three switches are provided in the upper left corner of the front panel which permit manual selection of the system clock source. During capture of video data from the scanning hardware, the external clock position must be selected. In this mode of operation the entire system is clocked and timed by use of the clock transmitted from the scanning hardware. This synchronizes the two systems and avoids further retiming hardware. The other two clock source buttons select internal clocks of two speeds. The HS (high speed) clock is

used for display of video data or execution of other programs at video rates. The MOS clock is a counted-down version of the HS clock and is used for lower-speed functions. Clock source selection may also be performed under program control.

The mode control buttons are located in the lower right portion of the control panel. These switches are used to command the system to operate in various ways. Instructions can be run, stepped, or repeated by use of the mode control buttons. A master SYSTEM RESET button is also included.

There are certain error conditions detectable by the MCU. If any of these conditions occur, all operation with the MCU is suspended and a fault light is enabled. After touching the SYSTEM RESET button, the contents of registers and memory locations may be examined and the cause of the fault determined, following which operation may (optionally) be resumed.

The last special function of the control panel is provided by the BOOTSTRAP button. This button is used only to initialize the system by initiating a special internal function which loads a logical record from magnetic tape into the program section of the FSM. This function greatly simplifies the overall operation of the ICAS, which is continued following BOOTSTRAP by the use of Tektronix 4051.

PERIPHERAL INTERFACES

In order for the memory and control system to communicate control and data information to peripheral devices, interface hardware is provided. There are four groups of interface hardware (not including the scanning hardware or the memory), each with multichannel capability. The peripheral interfaces currently implemented are the Versatec printer/plotter interface, the Kennedy magnetic tape interface, an RS-232 serial interface, and the (previously discussed) IEEE GPIB interface.

These interface channels (though relatively few in number) provide all the flexibility needed to perform the capture, storage, display, processing, and analysis of USPS video images.

In order to allow generation of hard copies of digitized images, the MCU includes an interface to a printer/plotter. The interface provides for image plotting of up to 8 million 1-bit pels per second transmitted as 8-bit bytes. The interface also provides for transmission of up to 1 million ASCII characters per second, which allows for hard copy of processed image statistics and processing programs.

Magnetic tape data transfers require a control register wider than the 8 bits of the other interfaces, and require block transfers of data. Therefore, the interfaces are considerably different from other parallel interfaces. The magnetic tape channel has the capability to communicate with four tape drives. Special control is provided to facilitate block transfers of data. Also included are standard command-register outputs and sense or status condition inputs from the magnetic tape unit to the control system.

In the RS-232 interface, data are transferred as 8-bit characters, bit-serial at 9600 baud. The MCU includes the serial-to-parallel, parallel-to-serial, and timing logic required. On the MCU side of the interface, data are 8-bit parallel and are accessed on the low-order 8 bits of the MCU I/O data bus.

The two major blocks not mentioned here are the memory interface which was discussed earlier and the microprogram control element which is discussed in the next section (the 3001 microprogram control unit).

SYSTEM SOFTWARE DESCRIPTION

MICROPROGRAM CONTROL

A crucial part of any digital logic system is the control sequence generator. This logic block is reponsible for maintaining system timing and synchronization. It generates all the control signals required by the remainder of the system. This control sequencer is responsible for directing the operation of all other logic blocks within the system. Methods of implementing this control hardware fall into two general categories. Older equipment generally used a sequential state counter approach in which the entire control structure is defined by hardwired logic elements. This is perfectly adequate for smaller logic systems or for those in which changes in the control structure will not be made. Extensive hardware rework may be required in this type of control structure if minor alterations in the sequence generator output states are required. A more versatile approach in which the control structure is stored as a bit pattern in a memory is called microprogramming. All that is required to completely alter the control structure of a microprogrammed machine is to reprogram the micromemory.

A microprogram is similar to machine or assembly language in that they are both logical sequences of instructions controlling the operation of the machine. The primary difference is that whereas an assembly language instruction might specify an ADD instruction and the main memory address of the data to be used, a microinstruction would specify the data paths and register controls as well as the ALU operation. In order to accomplish this, the state of all control signals required internal to the machine is stored in the micromemory. These control signals include data routing (bus enables and data sources), memory controls, clock controls, system status checks, and special function generation. The disposition of each hardware resource is controlled at all times by the micromemory, either explicitly by design or implicitly by omission.

There are a great number of implementation methods for microprogram control structures. There are possible variations in the organization of micromemory and the microword, in the coding and routing of control signals, and in the method of invoking the control signals. Regardless of the implementation method chosen, some form of micromemory address sequencer is necessary to select the order in which to execute microinstructions.

In the MCU hardware the microprogram address generator is an Intel 3001 microprogram control unit. Two separate microprogram memories are provided for control storage. One memory is a high-speed programmable read-only memory (PROM) which stores the controls required to manipulate data at video rates. This memory is supplemented by a smaller electrically alterable read-only memory (EAROM) which is used at lower speeds for microprogram development and testing and for operation at low speeds.

3001 MICROPROGRAM CONTROL UNIT

The Intel 3001 microprogram control unit contains a micromemory address register and the primary set of logic necessary to maintain proper microprogram sequencing (fig A43). The microprogram address register is a 9-bit register with outputs designated MA_8 through MA_0 (high-order to low-order bit). The contents of this register select one of 2^9 (512) possible micromemory locations. The register contents are synchronously determined by the

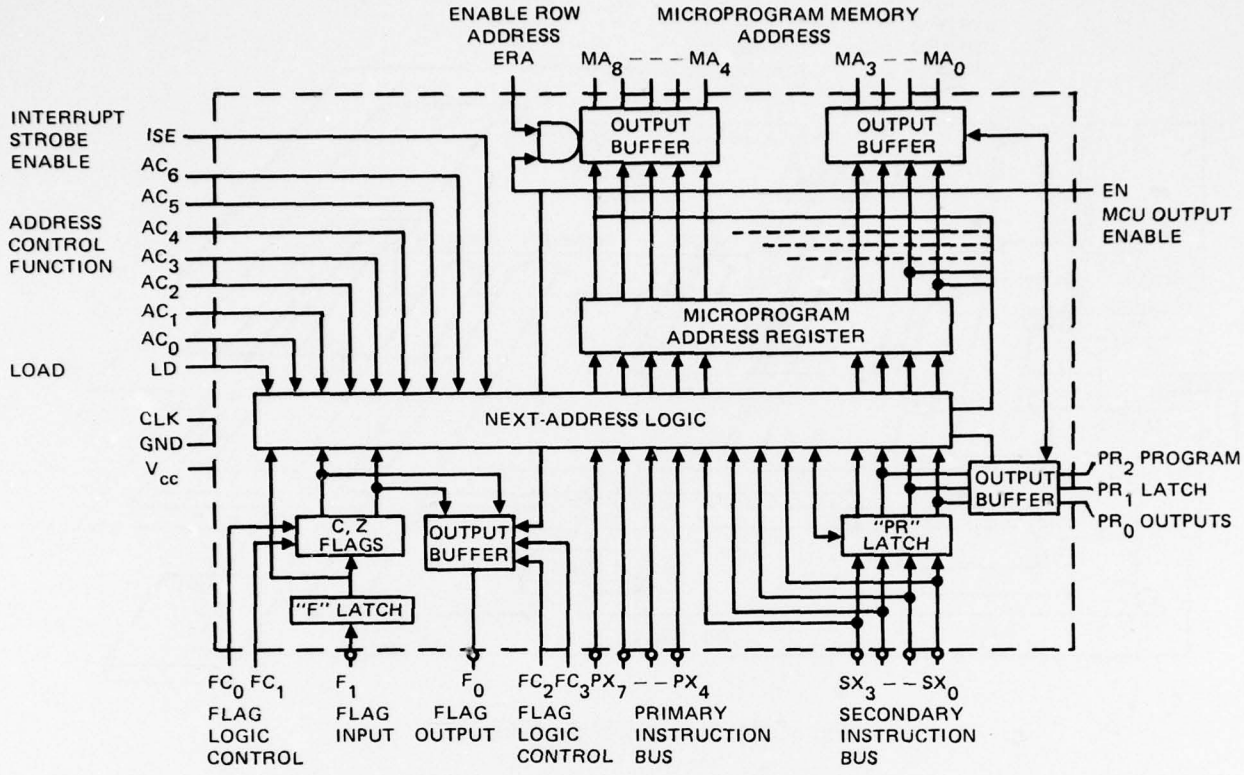


Figure A43. 3001 block diagram.

next-address logic in one of several ways. The low-order 8 bits of the register can be loaded from the primary and secondary instruction bus inputs (PX_7–SX_0) by setting the LD input to active high. After the rising edge of the clock, the data on the secondary instruction bus (SX_3 - SX_0) will be loaded into MA_7 through MA_4 and the data on the primary instruction bus (PX_7–PX_4) will be loaded into MA_3 through MA_0. On a LD operation, MA_8 is always set to a logic 0, allowing selection of any one of the first 256 locations in a 512-word micromemory. During normal microprogram execution, the next-address logic generates each successive microprogram address as a function of the current address and the address control function inputs (AC_6 through AC_0). As shown in figure A44, the AC values are stored in micromemory so that each microinstruction controls the sequencing to the next microinstruction. The 3001 contains two flags (C and Z) and a test input (F-latch) which may also affect the next micromemory address, depending upon the next-address function specified by AC_6 through AC_0. For a detailed description of this complicated operation, the reader is referred to the published Intel 3001 data sheet (ref A5).

Figure A44 shows the general interconnection and function of all microlevel components. In operation, each micromemory output word contains the appropriate controls for all hardware resources. Each sequence of microinstructions causes the system to perform some desired function called a macroinstruction. The starting micromemory address (called the opcode) for a particular macroinstruction is loaded into the microprogram address register by the LD function already mentioned. The address is obtained by a microprogrammed

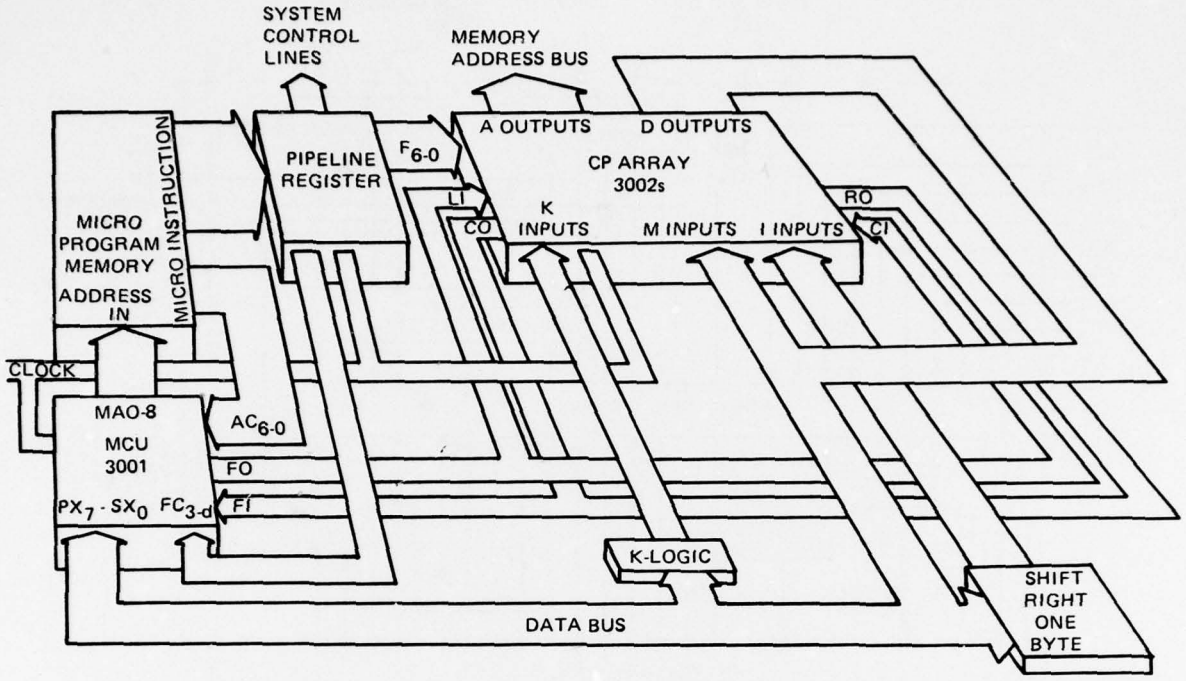


Figure A44. Microcontrol block diagram.

macroinstruction-fetch routine (fig A45), which checks for a front-panel operation and fetches a macroinstruction. The source for the opcode may be either the front-panel data switches or the main memory. By using main memory as the source of macroinstructions, a group of macroinstructions may be stored in memory in a logical sequence, constituting a macroprogram (or machine language program) and providing macrolevel control of the microprogram memory. There are currently two general types of macroinstructions implemented in the microprogram memory. The first type consists of the special-purpose microprograms to capture and display video data. The second type consists of a primitive instruction set allowing arithmetic and logic functions to be performed under macroprogram control.

An example of a typical operation would start at instruction $0F_H$. This sequence of microinstructions (fig A49) uses scratchpad register R_9 as a program counter and fetches from main memory an instruction from the location specified by R_9. If the instruction selected happened to be a "LDA" instruction (fig A50, opcode 80_H), then the microcode would jump from instruction $1D_H$ to instruction 80_H and proceed through the LDA routine. The last microinstruction of all macroinstructions must necessarily be a jump to the beginning of the fetch routine located at $0F_H$. In this manner a continuous fetch/execute sequence is implemented.

An appreciation of the complexity involved in the video operations can be gained by observing the flowchart of the capture microroutine (fig A46).

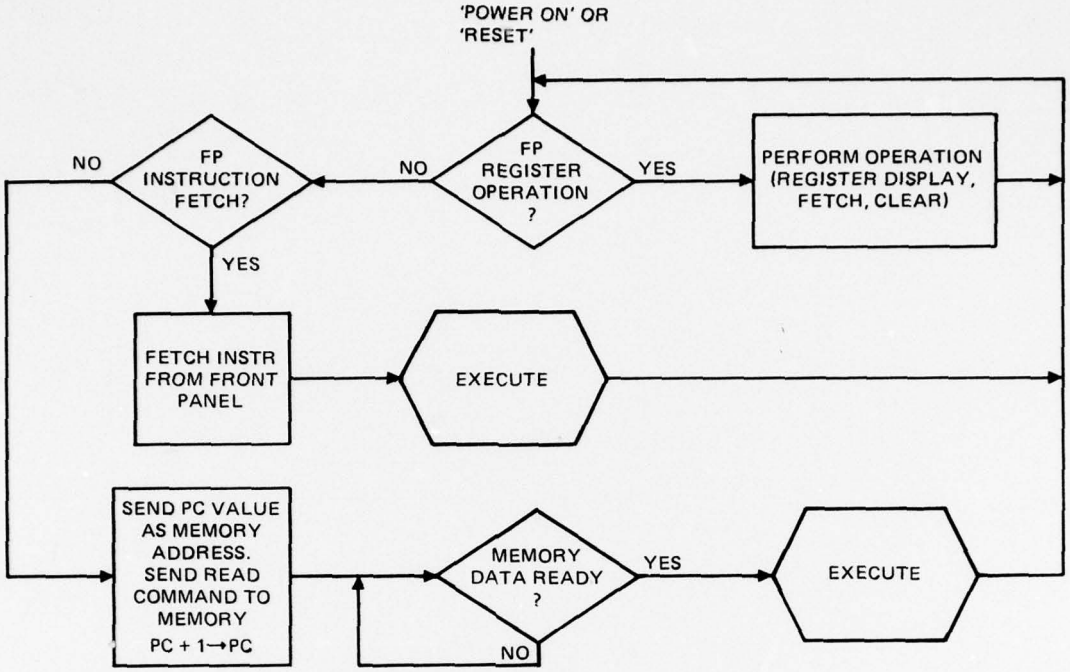
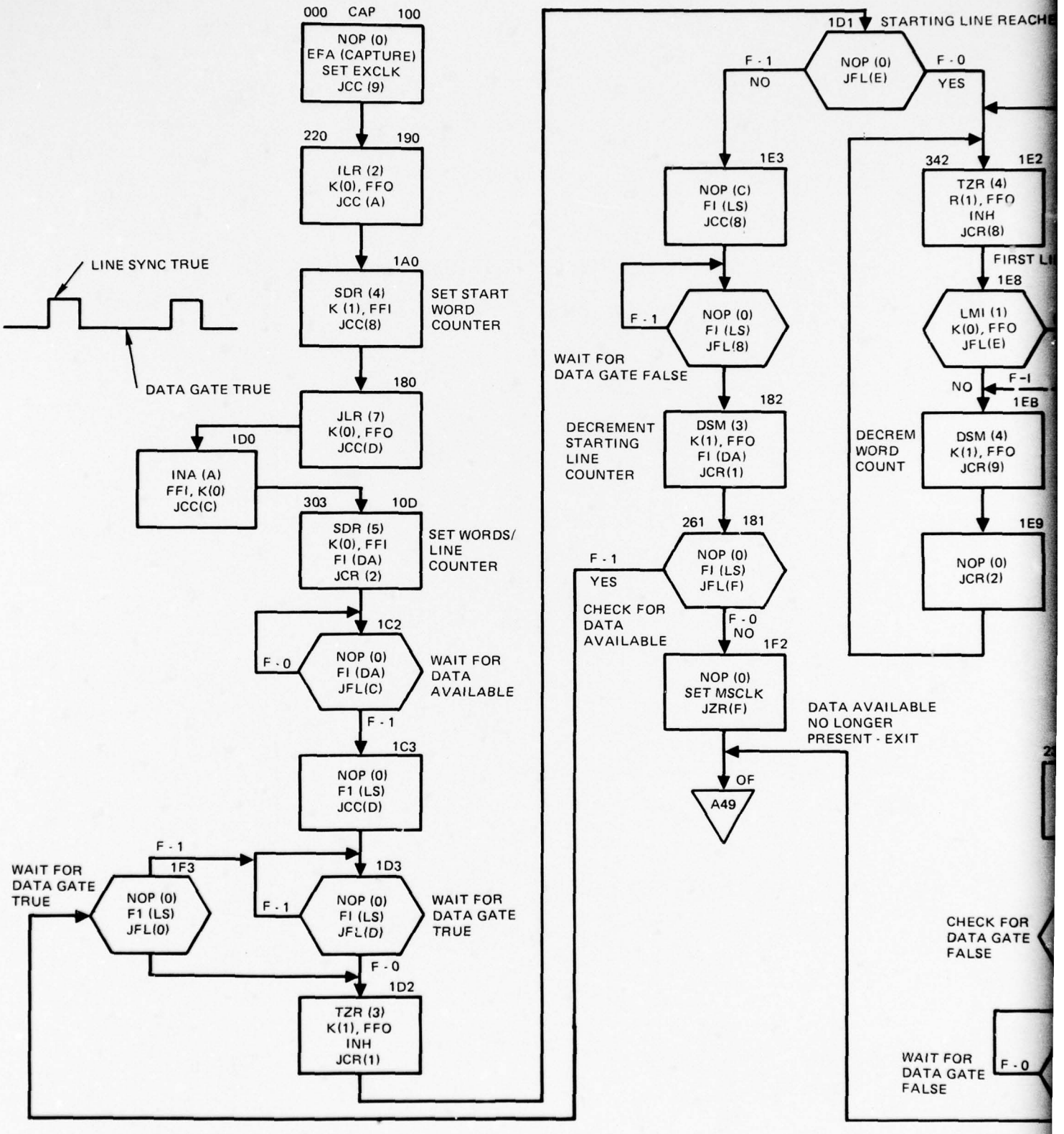


Figure A45. Microprogrammed fetch cycle.


000 CAP 100
NOP (0)
EFA (CAPTURE)
SET EXCLK
JCC (9)
220 190
ILR (2)
K(0), FFO
JCC (A)
LINE SYNC TRUE
1A0
SDR (4)
K (1), FFI
JCC(8)
SET START WORD COUNTER
DATA GATE TRUE
180
JLR (7)
K(0), FFO
JCC(D)
1D0
INA (A)
FFI, K(0)
JCC(C)
303 10D
SDR (5)
K(0), FFI
FI (DA)
JCR (2)
SET WORDS/ LINE COUNTER
1C2
F - 0
NOP (0)
FI (DA)
JFL(C)
WAIT FOR DATA AVAILABLE
F - 1
1C3
NOP (0)
F1 (LS)
JCC(D)
F - 1
1F3
WAIT FOR DATA GATE TRUE
NOP (0)
F1 (LS)
JFL(0)
1D3
F - 1
NOP (0)
FI (LS)
JFL(D)
WAIT FOR DATA GATE TRUE
F - 0
1D2
TZR (3)
K(1), FFO
INH
JCR(1)
1D1 STARTING LINE REACHE
F - 1
NO
NOP (0)
JFL(E)
F - 0
YES
1E3
NOP (C)
FI (LS)
JCC(8)
F - 1
NOP (0)
FI (LS)
JFL(8)
WAIT FOR DATA GATE FALSE
182
DECREMENT STARTING LINE COUNTER
DSM (3)
K(1), FFO
FI (DA)
JCR(1)
261 181
F - 1
YES
NOP (0)
FI (LS)
JFL(F)
CHECK FOR DATA AVAILABLE
F - 0
NO
1F2
NOP (0)
SET MSCLK
JZR(F)
DATA AVAILABLE NO LONGER PRESENT - EXIT
OF
A49
342 1E2
TZR (4)
R(1), FFO
INH
JCR(8)
FIRST LI
1E8
LMI (1)
K(0), FFO
JFL(E)
F - I
NO
1E8
DECREM WORD COUNT
DSM (4)
K(1), FFO
JCR(9)
1E9
NOP (0)
JCR(2)
CHECK FOR DATA GATE FALSE
WAIT FOR DATA GATE FALSE
F - 0

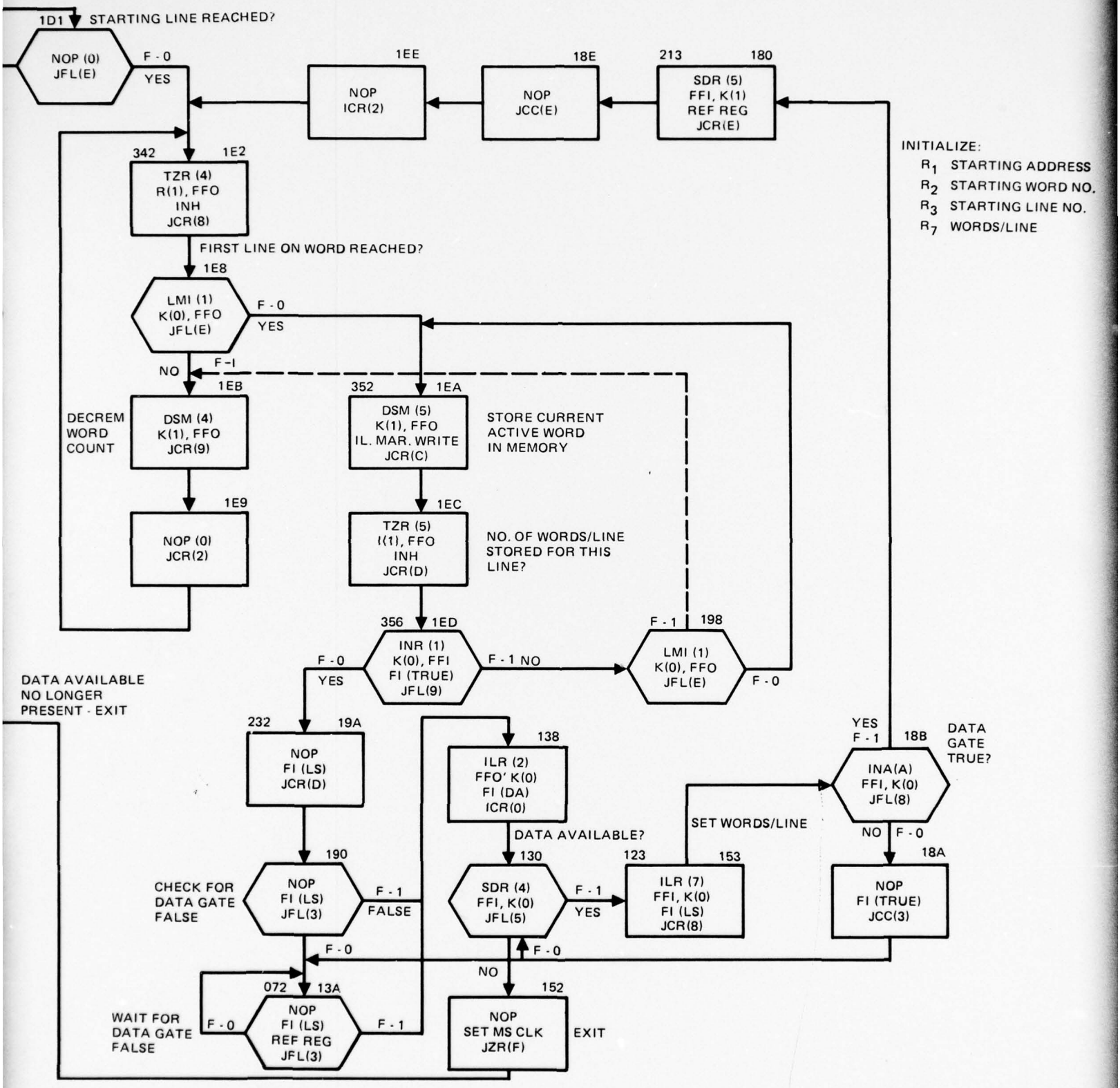


Figure A46. CAPTURE microprogram flowchart.

SPEED CONSIDERATIONS

As described earlier, the 3001 generates the address information for the micromemory. Speed considerations have made it necessary to separate the microinstruction memory into two separate modules. Micromemory 1 is a low-speed UV erasable MOS EAROM. Since this memory can be erased and reprogrammed repeatedly, it is used for program development and testing. Its 1-microsecond cycle time, however, is far too great to be useful for video routines. Micromemory 2 is a Schottky TTL PROM (with a 60-ns cycle time) which is not erasable. After video and other microroutines are tested and debugged in the MOS micromemory, they are permanently programmed into the TTL micromemory, where they operate at the required video rates.

The 3001 microcontrol unit applies its address output to both micromemories simultaneously (fig A47). At each system clock pulse the 3001 generates the next microaddress, and the current microinstruction is loaded into independent pipeline registers from each micromemory. The microinstructions stored in the pipeline registers are tristate-buffered to a single microinstruction bus and are selected by the system clock source. When the low-speed MOS clock is selected, the same signal enables instructions from the MOS memory onto the microinstruction bus. When high-speed operation is required, the high-speed (HS) or the external (EXT) clock is selected and micromemory 2 is enabled. The appropriate clock source flip-flop, and therefore micromemory selection, may be made either manually from the front panel or under program control via system control lines.

MICROCODE

Microcode is the term used for the organization of the individual microinstructions. The microcode implemented in the MCU uses a 48-bit microcontrol word divided into 14 control fields. (The fact that the control word is 48 bits long is coincidental and has no direct relationship to the 48-bit main memory word width.) Table A4 indicates the width of each control field and its use. Table A5 gives a breakdown of the field encoding scheme.

The control fields are decoded when appropriate and the resulting signals control the logic in the rest of the system. Strings or sequences of microcontrol words implement the more general macrolevel instructions. Using a program counter (R_9) and a microroutine (fetch) to read instructions from main memory, full programmability is achieved.

Figure A48 shows the format used in flowcharting microcode and figures A49 through A61 show the complete set of microprogrammed control routines implemented in the MCU. The flowcharts provide a detailed map of the microcode execution.

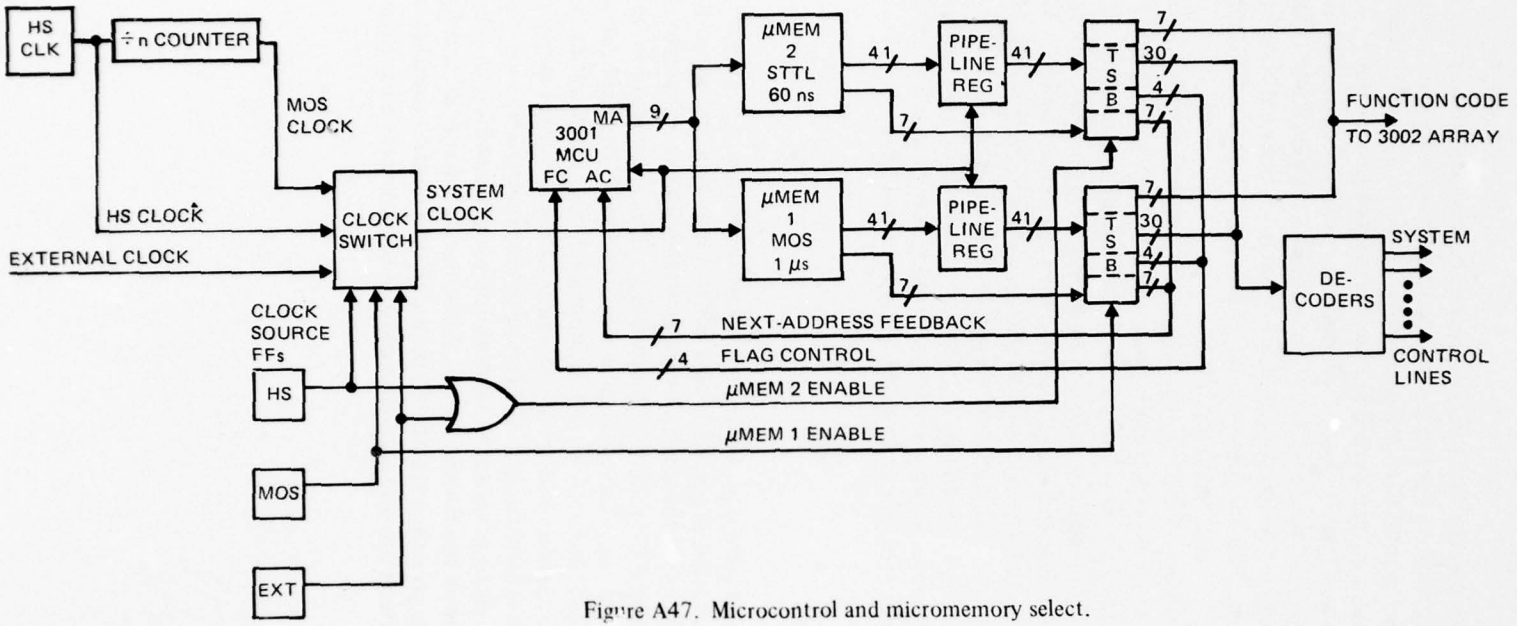


Figure A47. Microcontrol and micromemory select.

TABLE A4. MICROCODE CONTROL WORD FIELDS.

Control Word Bits	Field Width	Function
06-00	7	3001 next-address control
10-07	4	3001 flag control
17-11	7	3002 function code
19-18	2	K logic control
22-20	3	Bus data source control, MDB
25-23	3	Bus data source control, SDB
27-26	2	Main memory command
29-28	2	Clock source control
30	1	3002 clock inhibit
34-31	4	External function A
38-35	4	External function B
40-39	2	Address bus data source
45-41	5	Test input select
46	1	Test sense inversion
47	1	Spare

TABLE A5. MICROINSTRUCTION FIELD DECODE.

Field	μ-word bits	Code (Binary)	Function
AC	06-00	–	See 3001 data sheet (next address)
FC	10-07	–	See 3001 data sheet (flag control)
F	17-11	–	See 3002 data sheet (function code)
K	19-18	0 0	K = all 0's
		0 1	$K = K_x$*
		1 0	
		1 1	K = all 1's
MDB enables	22-20	0 0 0	NOP
		0 0 1	AC → MDB
		0 1 0	
		0 1 1	
		1 0 0	
		1 0 1	
		1 1 0	
		1 1 1	SBD → MDB
SDB enables	25-23	0 0 0	NOP
		0 0 1	Memory → SDB
		0 1 0	Input Logic → SDB
		0 1 1	Tape SDB
		1 0 0	Data Switches → SDB
		1 0 1	Aux I/O → SDB
		1 1 0	
		1 1 1	MDB → SDB
Memory Control	27-26	0 0	NOP
		0 1	WRITE
		1 0	READ
		1 1	REFRESH REQUEST
Clock Control	29-28	0 0	NOP
		0 1	Set HS Clk-Enable TTL m
		1 1	Set MS Clk-Enable MOS m
		1 0	Set EX Clk-Enable TTL m
CK INH	30	0	NOP
		1	Inhibit CPE clock

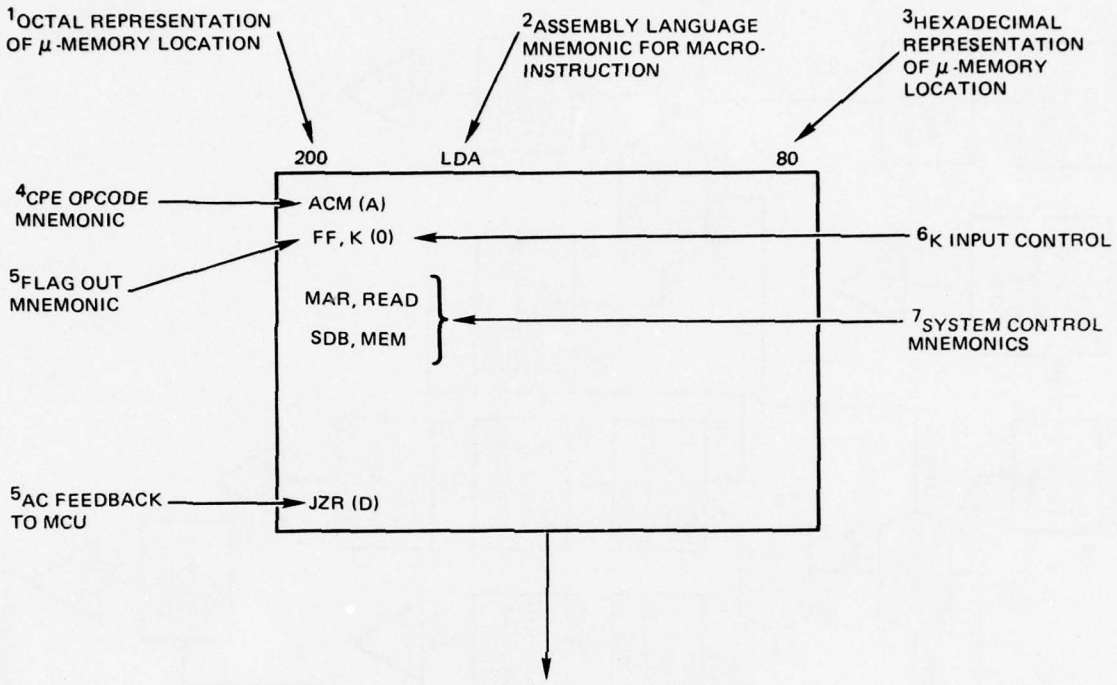
*x specified by $EFB_{1,0}$

TABLE A5. MICROINSTRUCTION FIELD DECODE. (Continued).

Field	μ-word bits	Code (Binary)	Function
External Function A	34-31	0 0 0 0	NOP
		0 0 0 1	Set "Step Macro"
		0 0 1 0	Capture
		0 0 1 1	
		0 1 0 0	
		0 1 0 1	Clear Front Panel
		0 1 1 0	IR (R_n)
		0 1 1 1	IR (Sense)
		1 0 0 0	Vertical Sync
		1 0 0 1	IR (K_n)
		1 0 1 0	I/O Strobe (IOS)
		1 0 1 1	Boot Done
		1 1 0 0	
		1 1 0 1	
		1 1 1 0	
		1 1 1 1	
External Function B	38-35	0 0 0 0	NOP
		0 0 0 1	Display Cycle Start (DCS)
		0 0 1 0	SPX - MDB
		0 0 1 1	N → F0, 3
		0 1 0 0	SPX - IR
		0 1 0 1	Memory Protect (M PROT)
		0 1 1 0	Data available out (DAO)
		0 1 1 1	Boot TAPE
		1 0 0 0	Horizontal sync
		1 0 0 1	Data Ready for TAPE (DRT)
		1 0 1 0	Load Tape Data Register (LTDR)
		1 0 1 1	
		1 1 0 0	
		1 1 0 1	
		1 1 1 0	
		1 1 1 1	
MARB	40-39	0 0	NOP
		0 1	
		1 0	MAR → MARB
		1 1	MDB → MARB (MDBM)

TABLE A5. MICROINSTRUCTION FIELD DECODE. (Continued).

Field	μ-word bits	Code (Binary)	Function
TEST ENABLE	45-41	00000	CO/RO
		00001	SENSE 1
		00010	SENSE 2
		00011	SENSE 3
		00100	SENSE 4
		00101	SENSE 5
		00110	SCANNER DA (DA)
		00111	MAN FI
		01000	TRUE
		01001	MDB_{47}
		01010	RUN
		01011	Flag out
		01100	LINE SYNC (Scanner) (LS)
		01101	R_n
		01110	DSR_{24}
		01111	MDB_0
		10000	I/O status
		10001	WAIT (tape)
		10010	Tape gap detected (TGD)
		10011	Read data strobe (RDS)
		10100	BOOT EN
		10101	
		10110	
		10111	
		11000	
		11001	
		11010	
		11011	
		11100	
		11101	
		11110	
		11111	



NOTES:

1. OPTIONAL AND USUALLY APPEARS ONLY AT FIRST MICROWORD OF A MACROINSTRUCTION
2. APPEARS ONLY AT FIRST MICROWORD OF A MACROINSTRUCTION
3. LEADING ZERO NOT GIVEN FOR FIRST 256 LOCATIONS
4. SEE 3002 DATA SHEET FOR FUNCTION. PARENTHESES INDICATE REGISTER OPERATED UPON
5. SEE 3001 DATA SHEET FOR FUNCTION
6. SEE TABLE A5 FOR FUNCTION DESCRIPTION
7. FLAG INPUT IS SPECIFIED ONLY IF OTHER THAN THE DEFAULT CONDITION HCZ AND THEN APPEARS ON THE SAME LINE WITH FLAG OUT AND K-CONTROL

DEFAULT CONDITIONS (IF NOT SPECIFIED ON FLOWCHART)

FLAG IN – HCZ
SYSTEM CONT – NOP
TEST MUX – CO/RO NONINVERTED

Figure A48. ROM flowchart format.

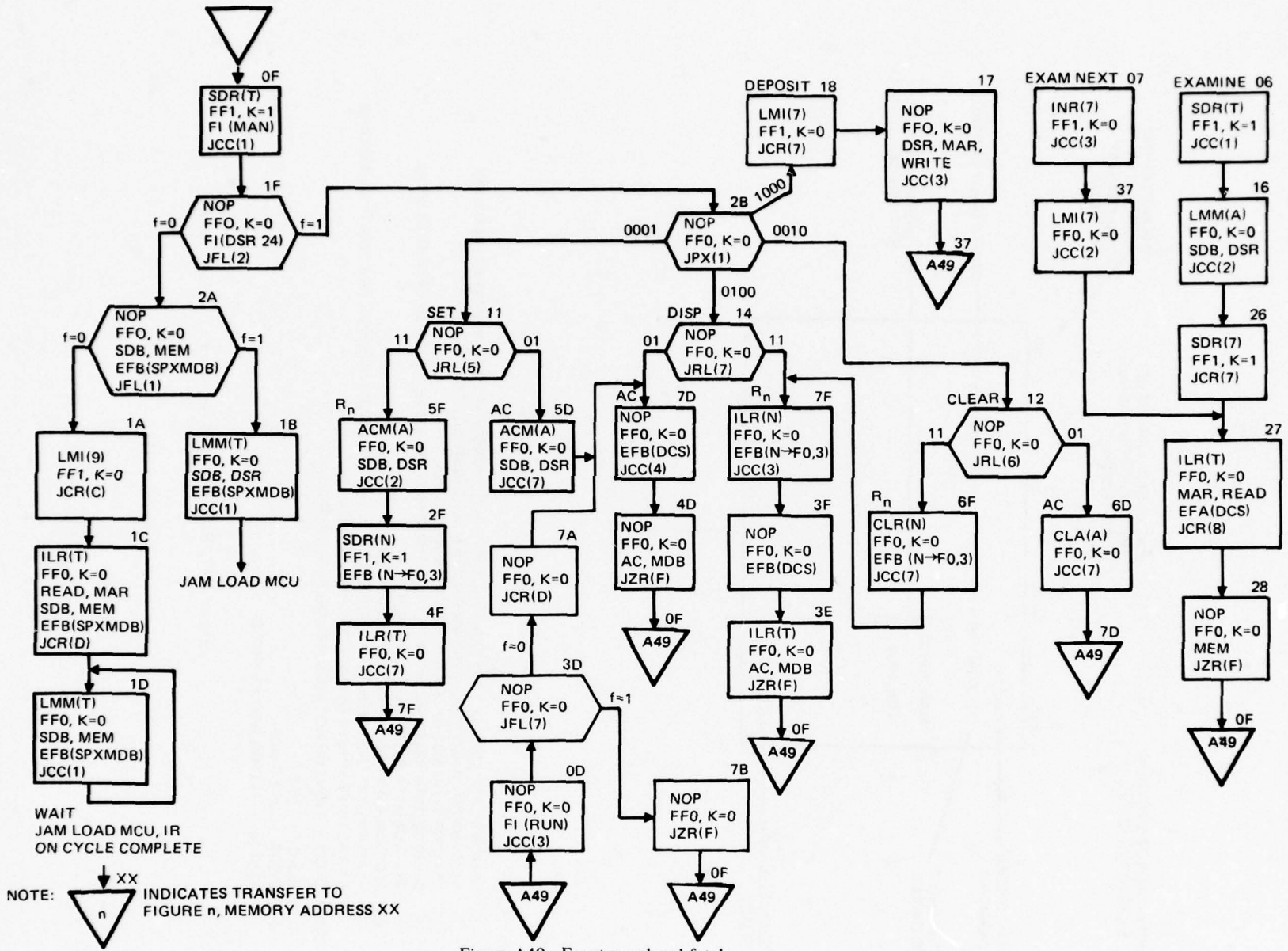
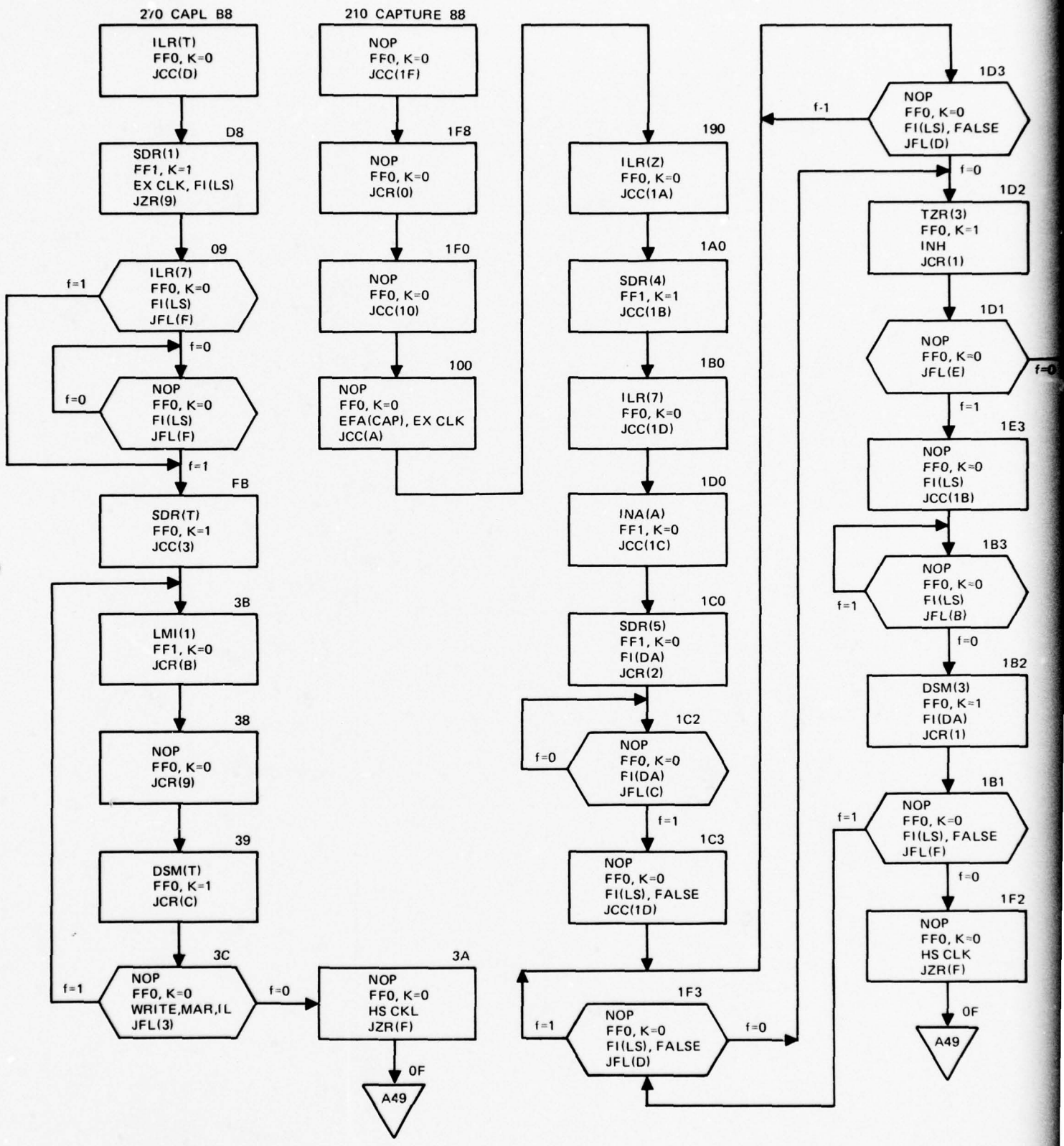


Figure A49. Front panel and fetch.


270 CAPL B8
ILR(T)
FF0, K=0
JCC(D)
D8
SDR(1)
FF1, K=1
EX CLK, FI(LS)
JZR(9)
09
ILR(7)
FF0, K=0
FI(LS)
JFL(F)
f=1
f=0
NOP
FF0, K=0
FI(LS)
JFL(F)
f=0
f=1
FB
SDR(T)
FF0, K=1
JCC(3)
3B
LMI(1)
FF1, K=0
JCR(B)
38
NOP
FF0, K=0
JCR(9)
39
DSM(T)
FF0, K=1
JCR(C)
3C
NOP
FF0, K=0
WRITE,MAR,IL
JFL(3)
f=1
f=0
3A
NOP
FF0, K=0
HS CKL
JZR(F)
0F
A49
210 CAPTURE 88
NOP
FF0, K=0
JCC(1F)
1F8
NOP
FF0, K=0
JCR(0)
1F0
NOP
FF0, K=0
JCC(10)
100
NOP
FF0, K=0
EFA(CAP), EX CLK
JCC(A)
190
ILR(Z)
FF0, K=0
JCC(1A)
1A0
SDR(4)
FF1, K=1
JCC(1B)
1B0
ILR(7)
FF0, K=0
JCC(1D)
1D0
INA(A)
FF1, K=0
JCC(1C)
1C0
SDR(5)
FF1, K=0
FI(DA)
JCR(2)
1C2
NOP
FF0, K=0
FI(DA)
JFL(C)
f=0
f=1
1C3
NOP
FF0, K=0
FI(LS), FALSE
JCC(1D)
1F3
NOP
FF0, K=0
FI(LS), FALSE
JFL(D)
f=1
f=0
1D3
NOP
FF0, K=0
FI(LS), FALSE
JFL(D)
f-1
f=0
1D2
TZR(3)
FF0, K=1
INH
JCR(1)
1D1
NOP
FF0, K=0
JFL(E)
f=0
f=1
1E3
NOP
FF0, K=0
FI(LS)
JCC(1B)
1B3
NOP
FF0, K=0
FI(LS)
JFL(B)
f=1
f=0
1B2
DSM(3)
FF0, K=1
FI(DA)
JCR(1)
1B1
NOP
FF0, K=0
FI(LS), FALSE
JFL(F)
f=1
f=0
1F2
NOP
FF0, K=0
HS CLK
JZR(F)
0F
A49

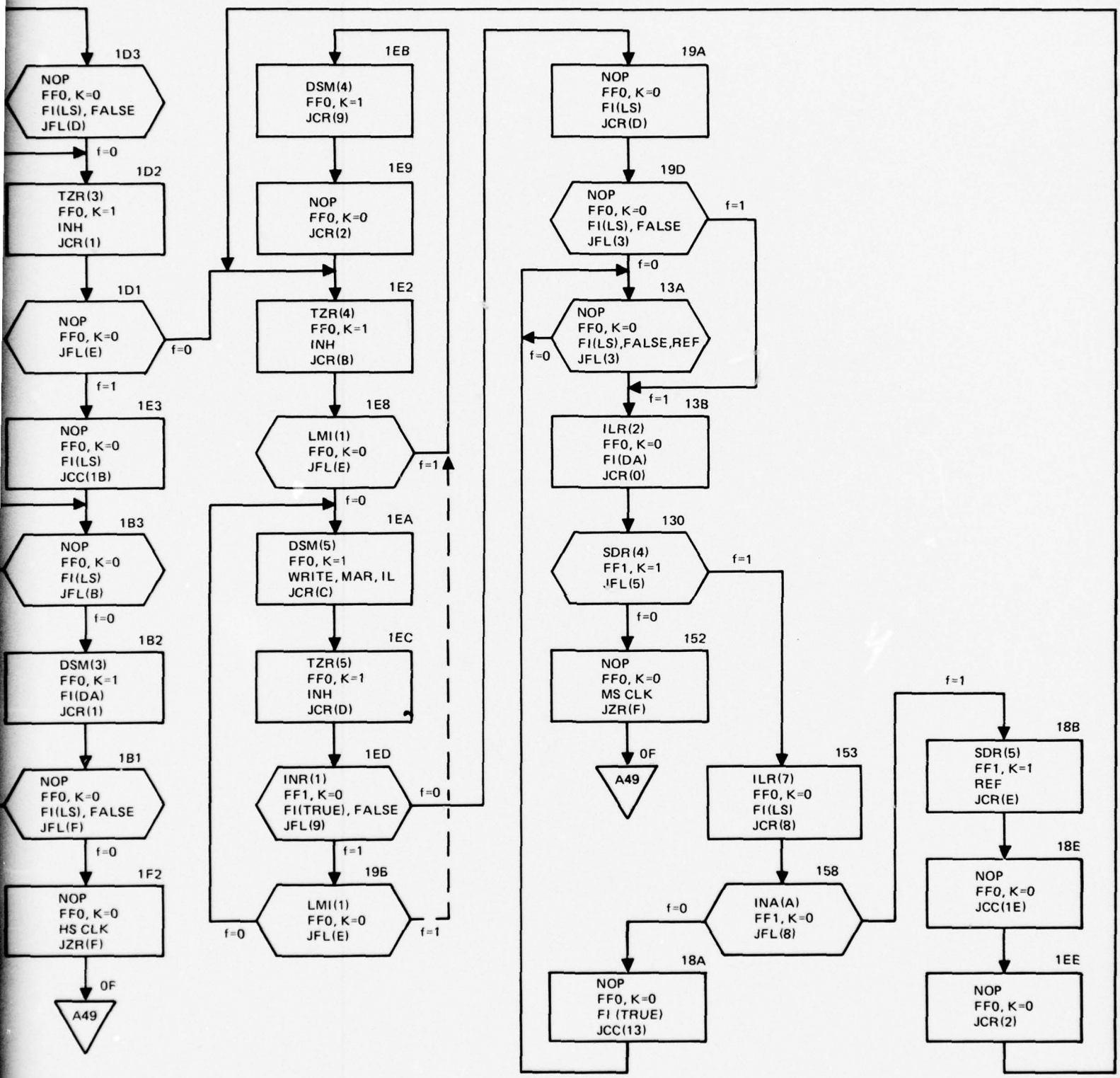


Figure A50. Capture instructions.

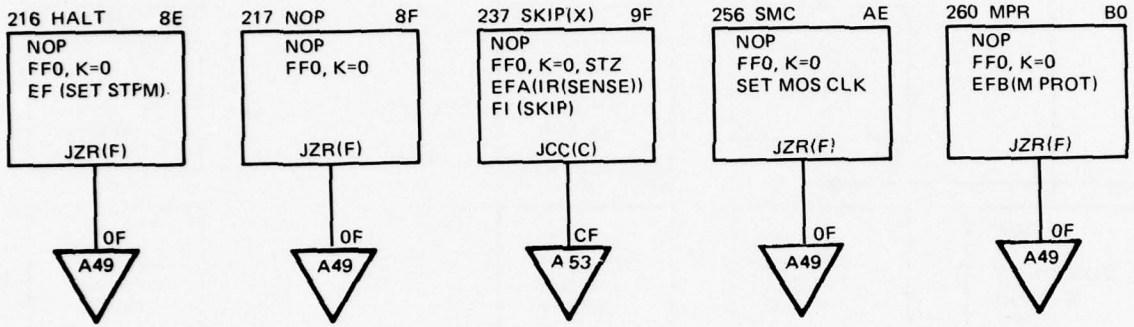


Figure A51. Miscellaneous instructions.

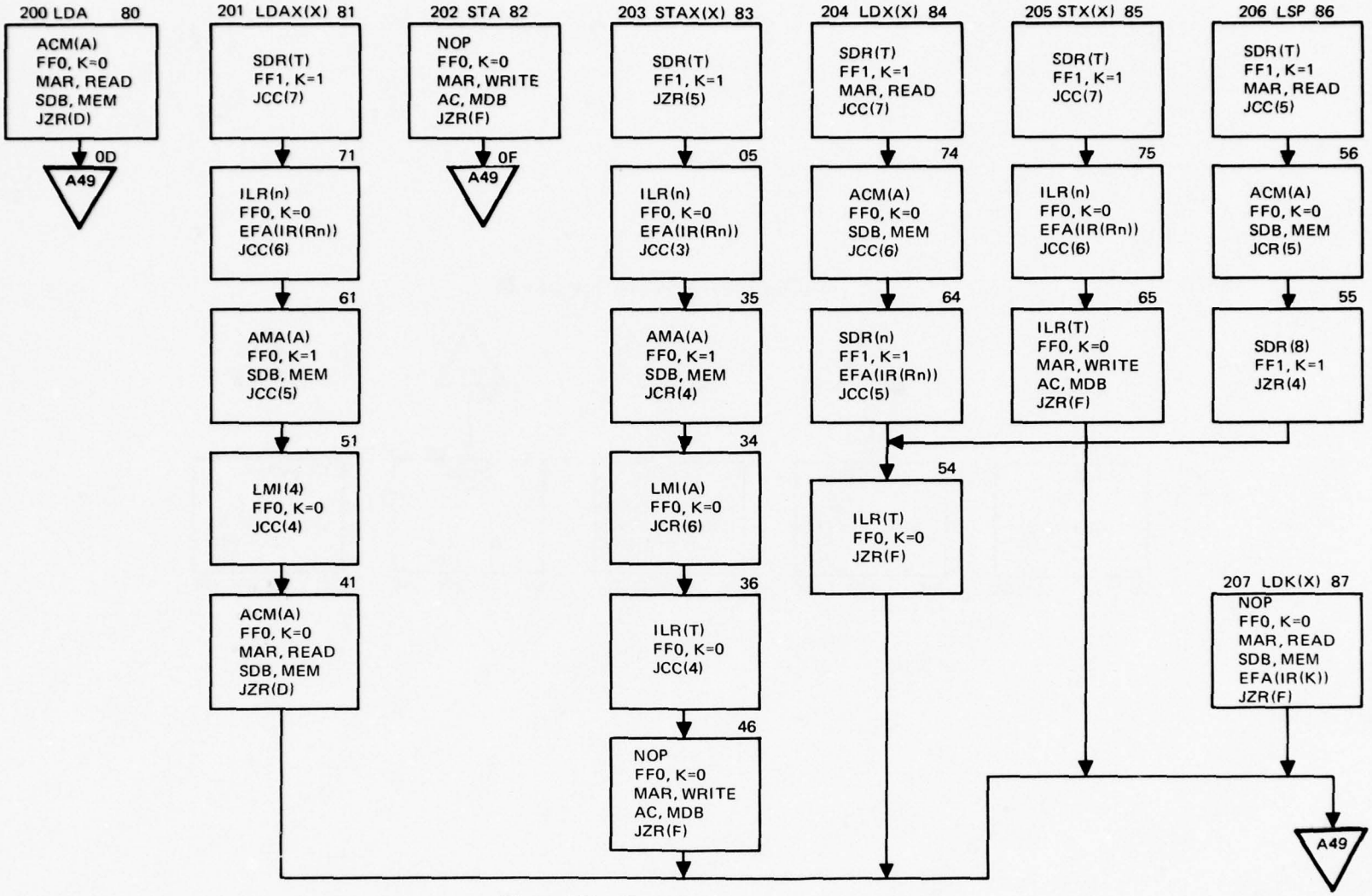


Figure A52. Memory reference instructions.

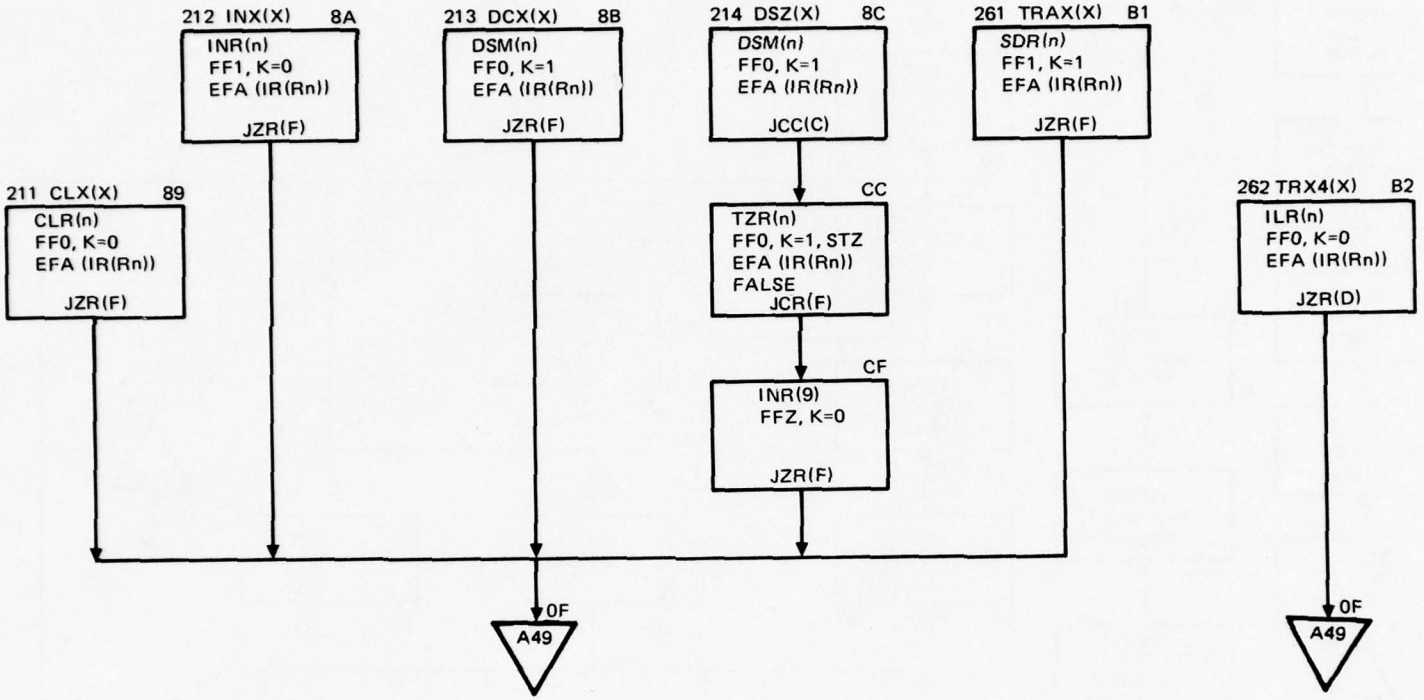


Figure A53. Register instructions.

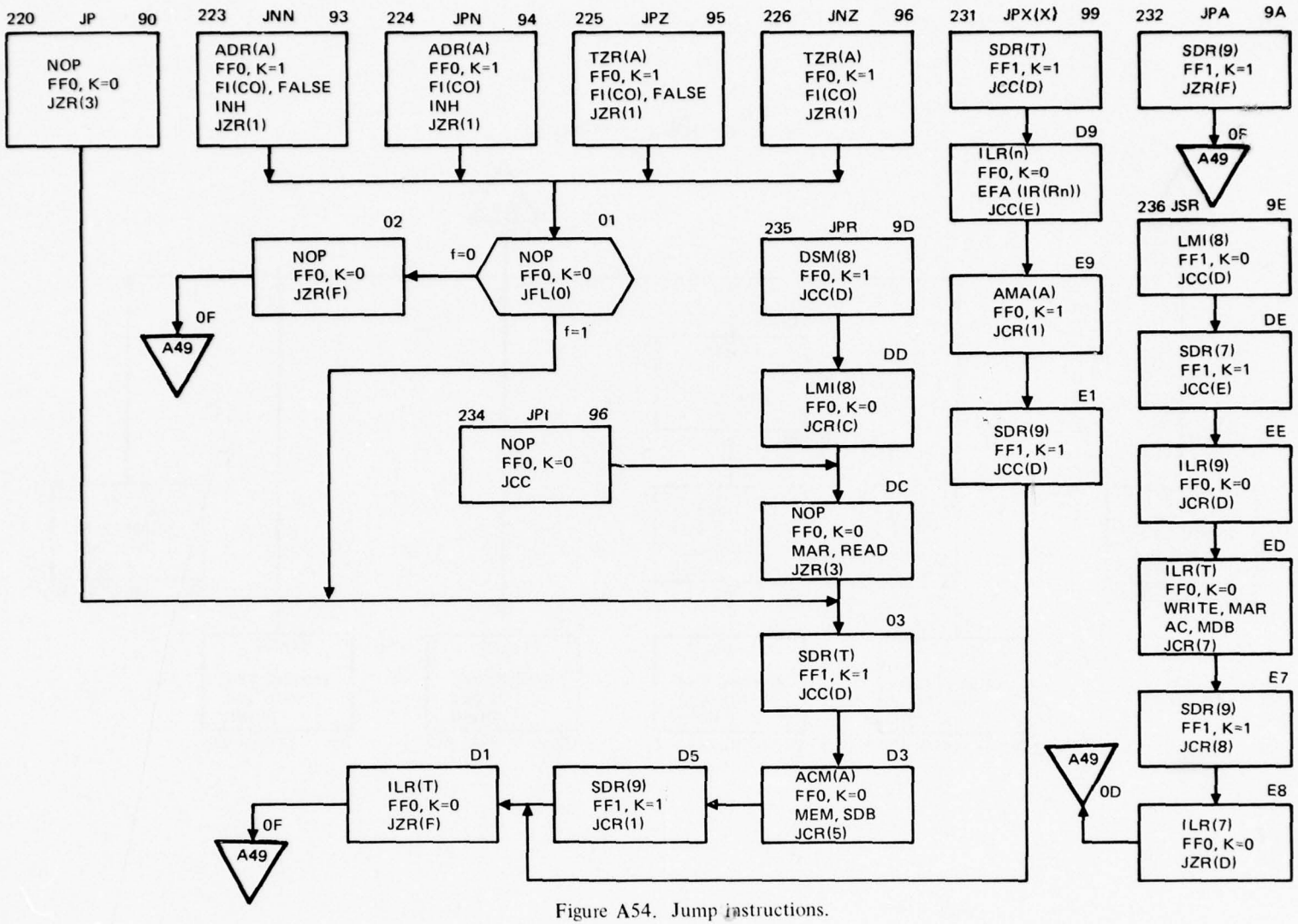


Figure A54. Jump instructions.

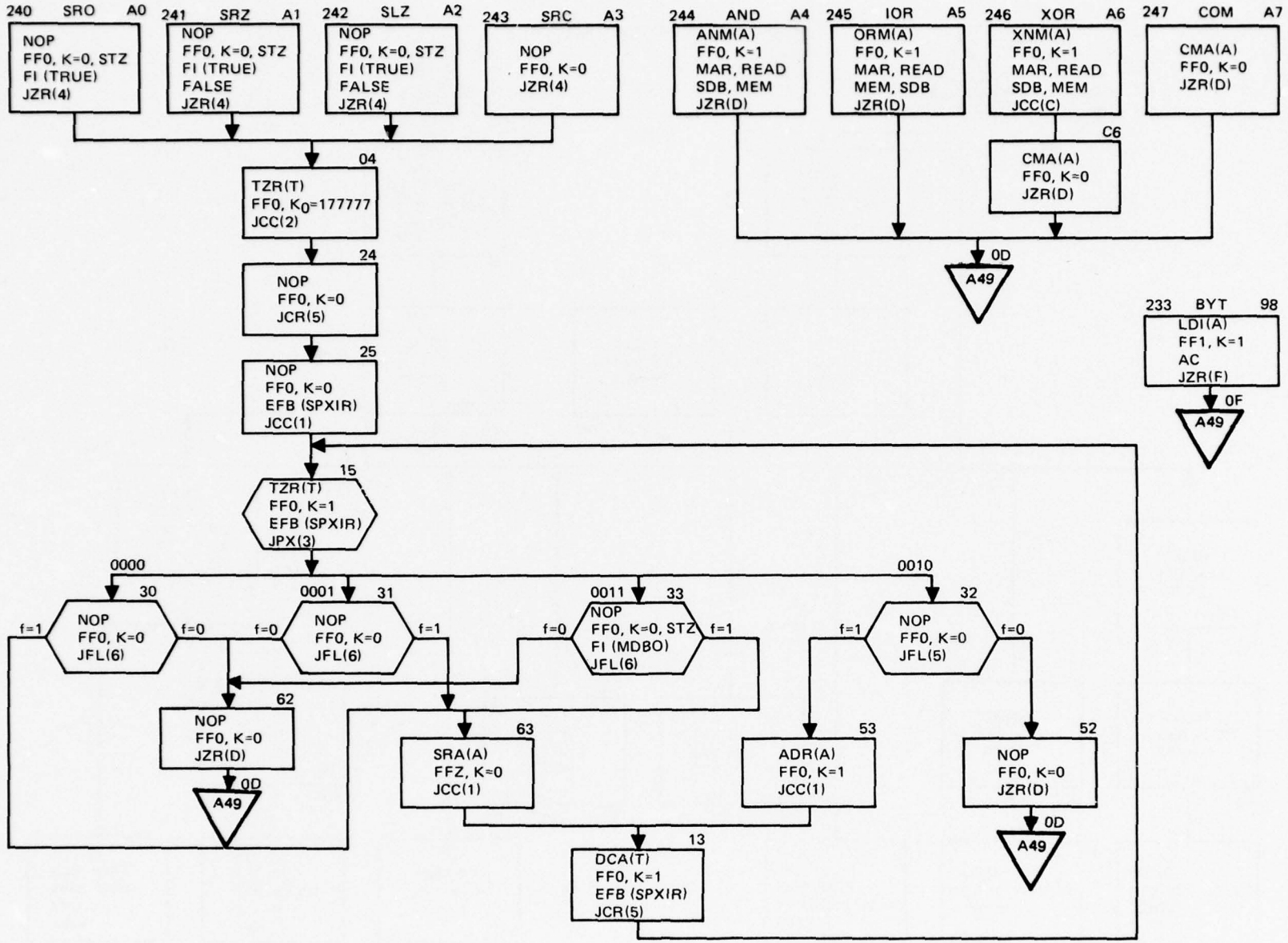


Figure A55. ALU instructions – A.

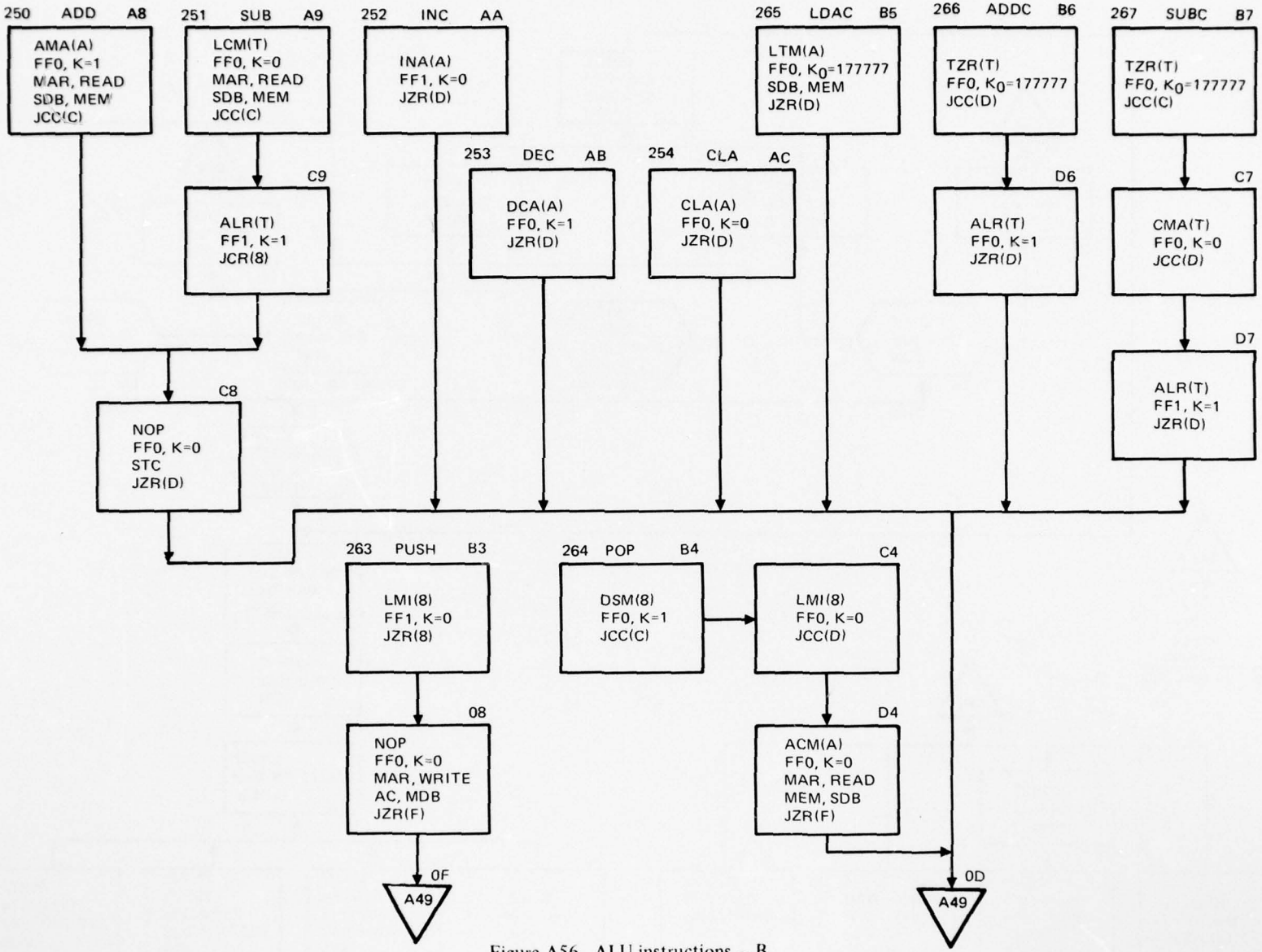


Figure A56. ALU instructions – B.

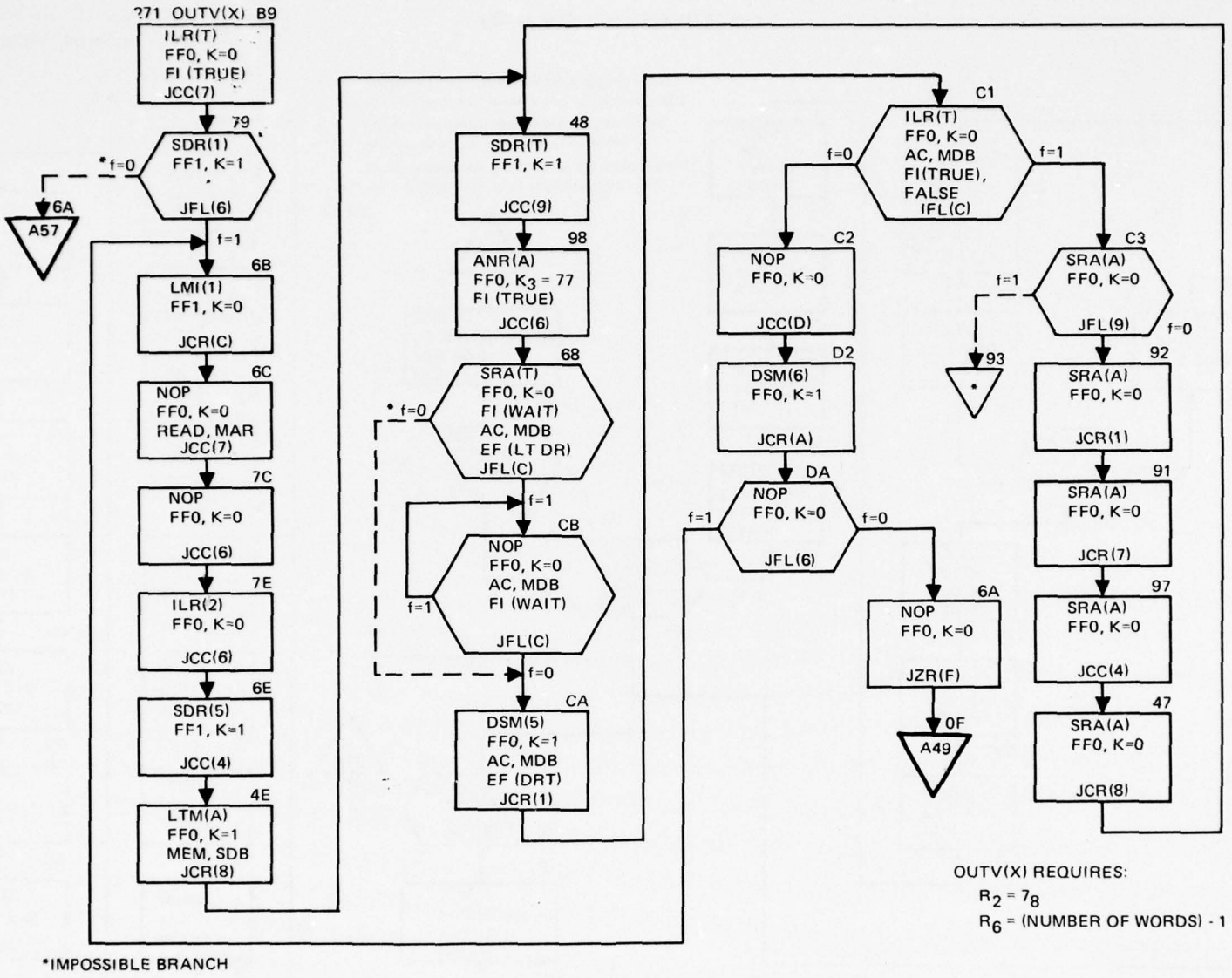


Figure A57. Video output to tape.

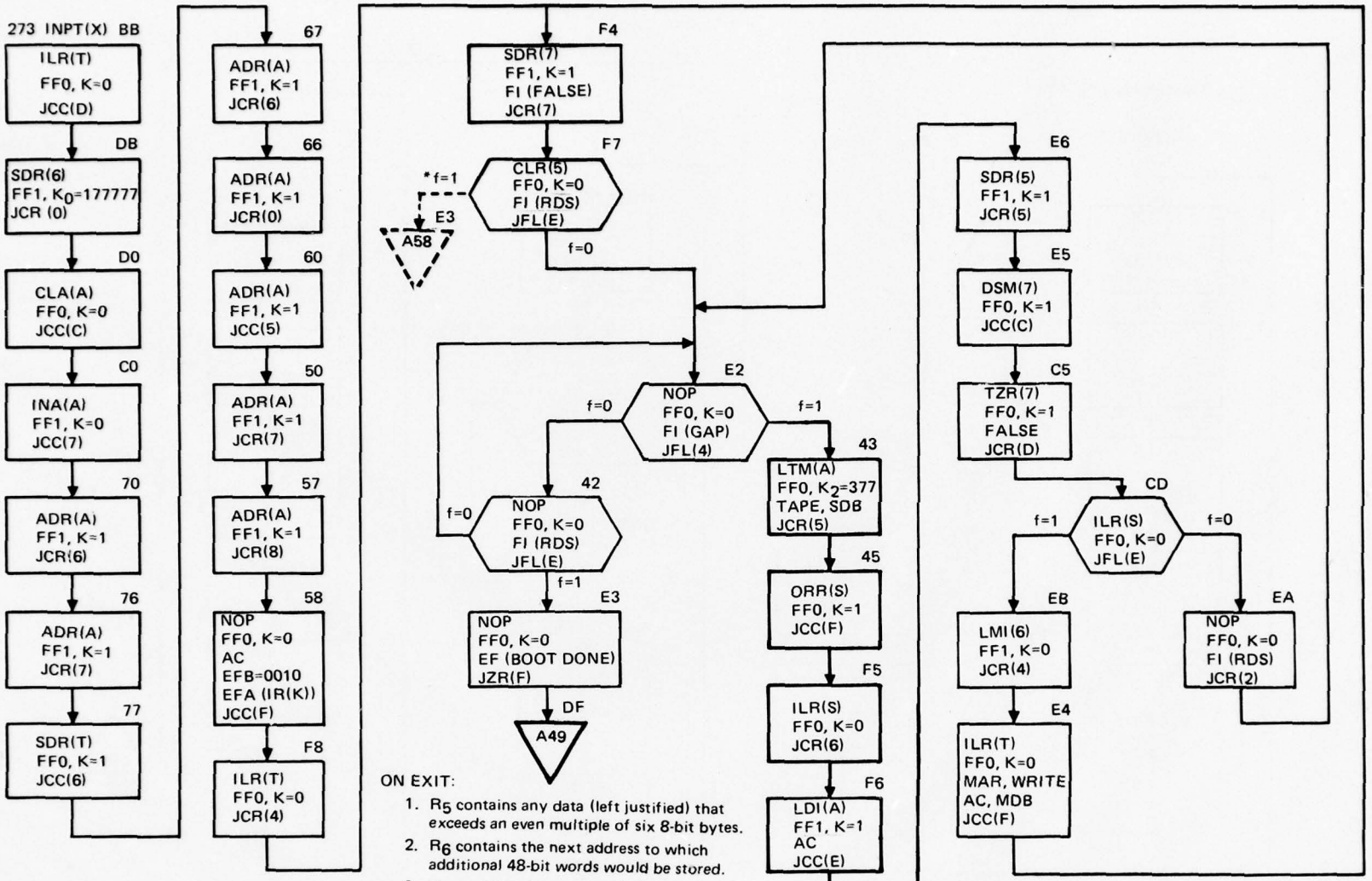


Figure A58. I/O instructions -- A.

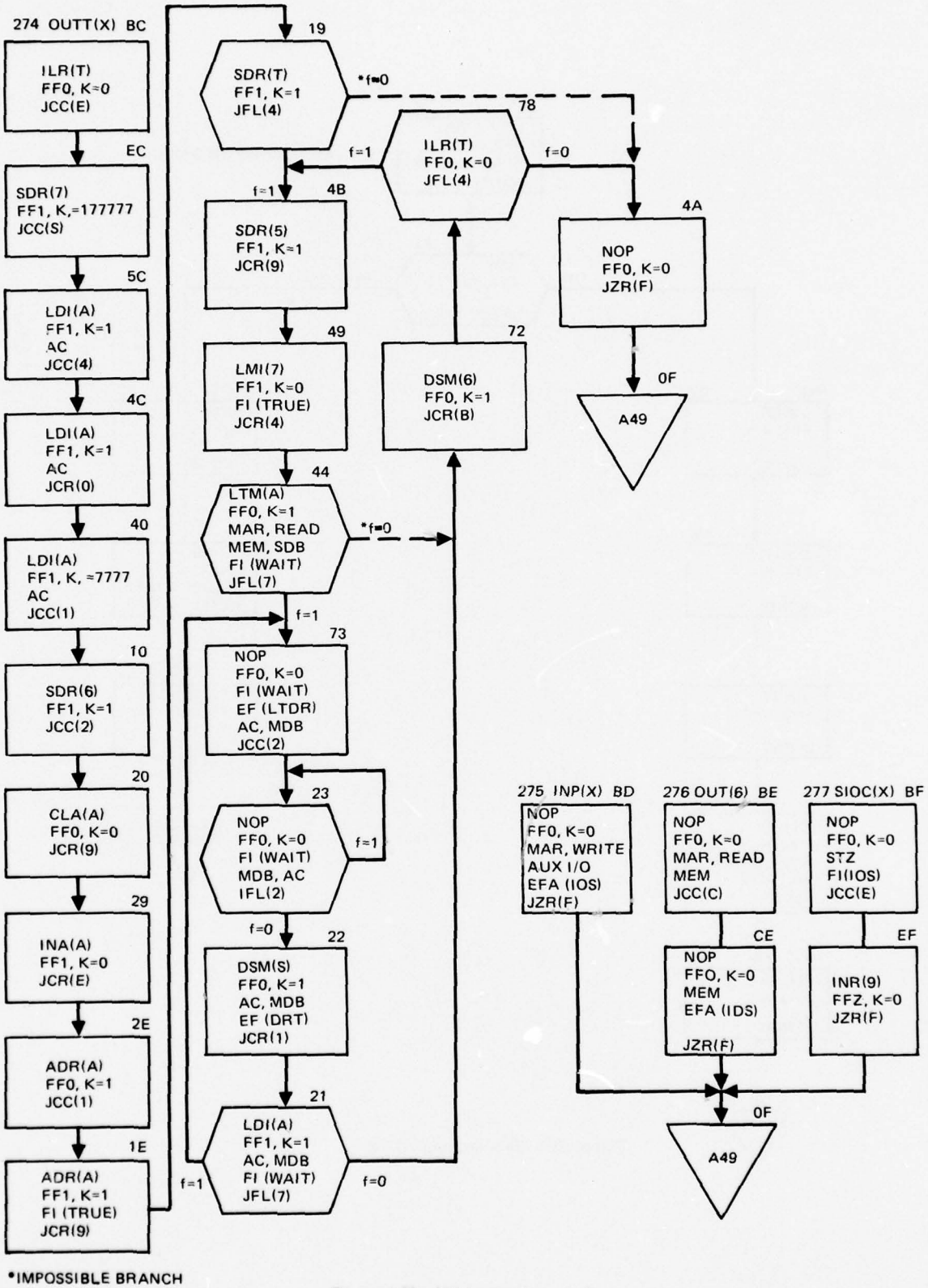


Figure A59. I/O instructions – B.

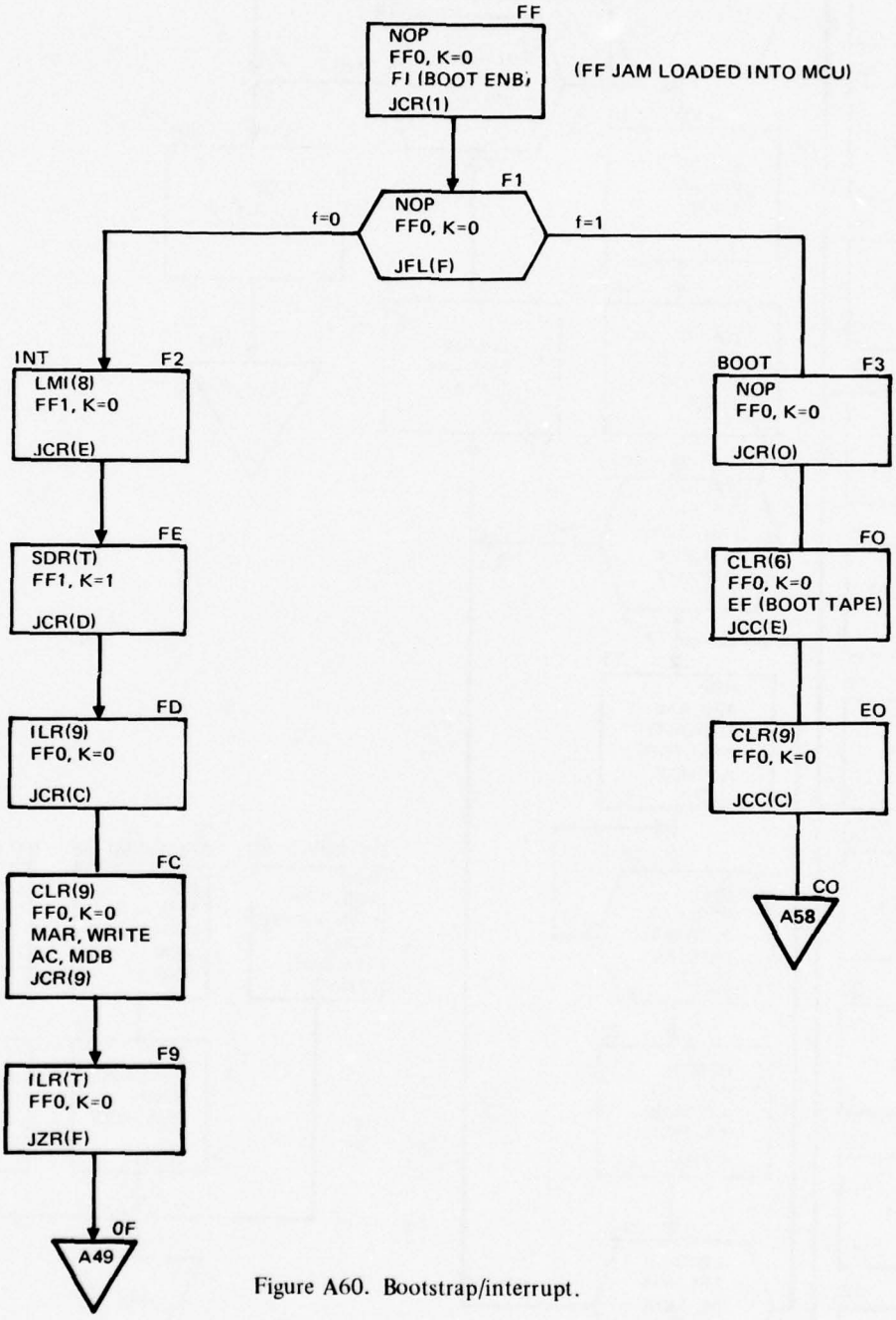
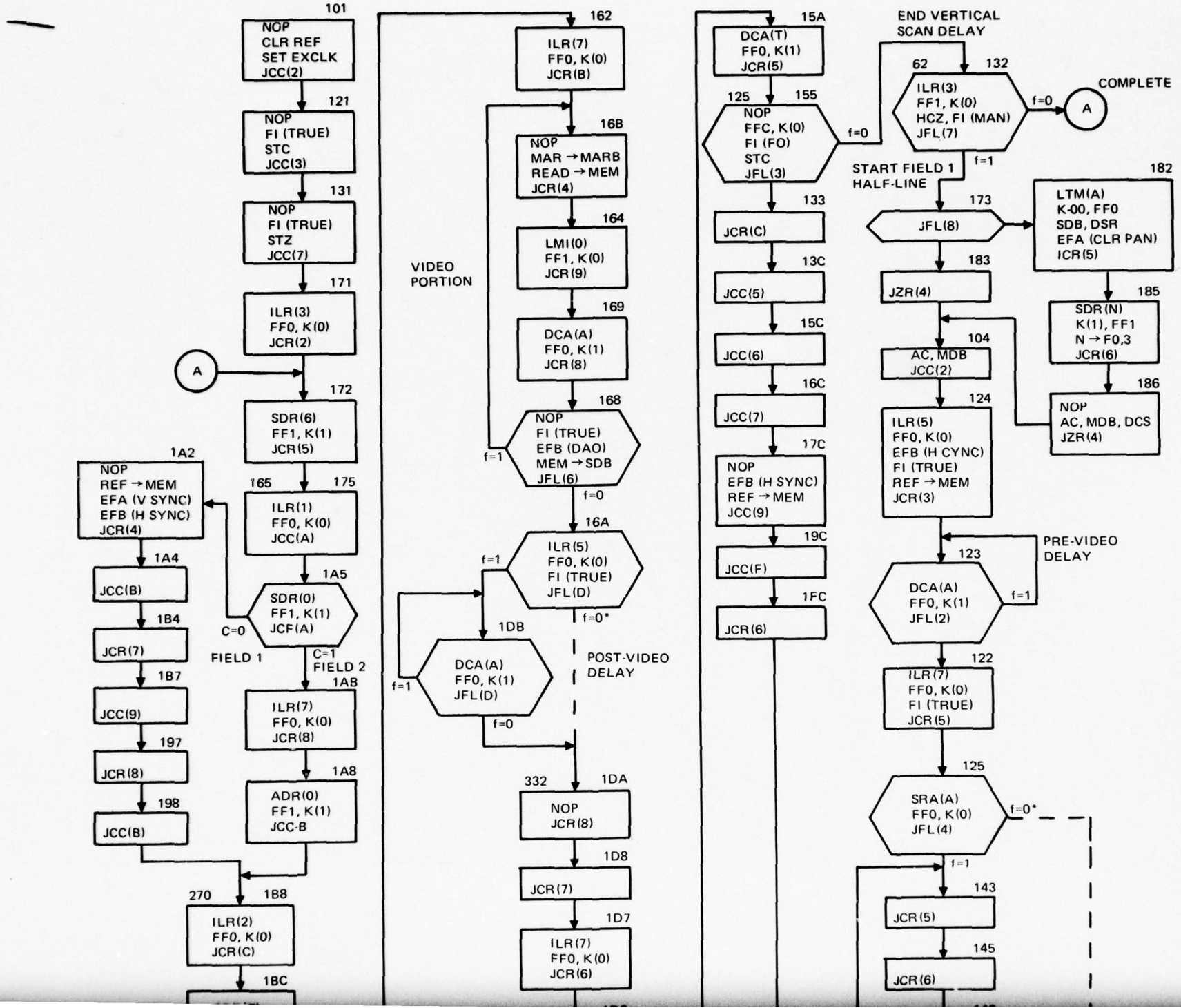
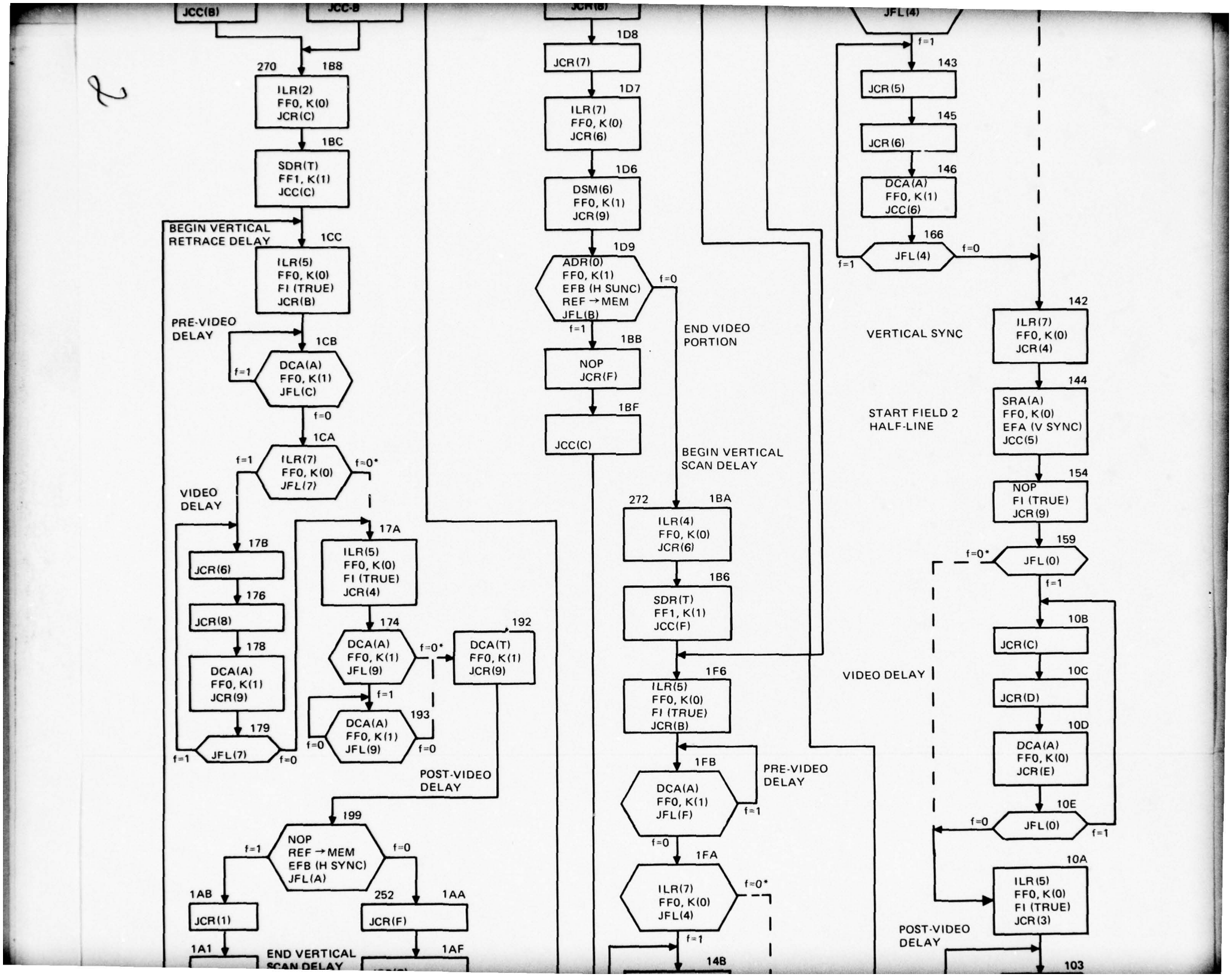
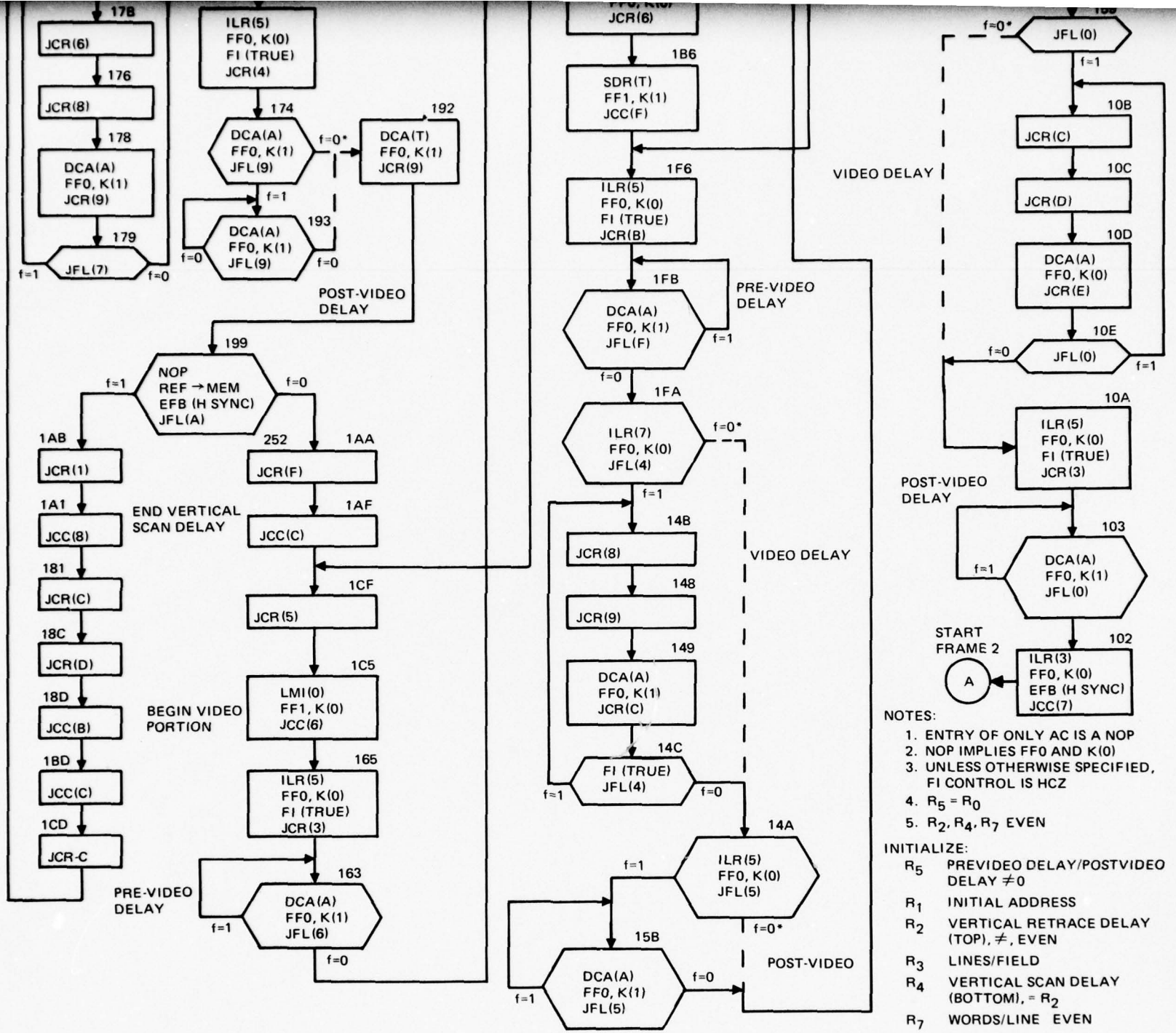


Figure A60. Bootstrap/interrupt.


101
NOP
CLR REF
SET EXCLK
JCC(2)
121
NOP
FI (TRUE)
STC
JCC(3)
131
NOP
FI (TRUE)
STZ
JCC(7)
171
ILR(3)
FF0, K(0)
JCR(2)
A
172
SDR(6)
FF1, K(1)
JCR(5)
1A2
NOP
REF → MEM
EFA (V SYNC)
EFB (H SYNC)
JCR(4)
165
175
ILR(1)
FF0, K(0)
JCC(A)
1A4
JCC(B)
1A5
SDR(0)
FF1, K(1)
JCF(A)
C=0
FIELD 1
C=1
FIELD 2
1B4
JCR(7)
1AB
ILR(7)
FF0, K(0)
JCR(8)
1B7
JCC(9)
1A8
ADR(0)
FF1, K(1)
JCC-B
197
JCR(8)
198
JCC(B)
270
1B8
ILR(2)
FF0, K(0)
JCR(C)
1BC
VIDEO
PORTION
162
ILR(7)
FF0, K(0)
JCR(B)
16B
NOP
MAR → MARB
READ → MEM
JCR(4)
164
LMI(0)
FF1, K(0)
JCR(9)
169
DCA(A)
FF0, K(1)
JCR(8)
168
NOP
FI (TRUE)
EFB (DAO)
MEM → SDB
JFL(6)
f=1
f=0
16A
ILR(5)
FF0, K(0)
FI (TRUE)
JFL(D)
f=1
f=0*
1DB
DCA(A)
FF0, K(1)
JFL(D)
f=1
f=0
POST-VIDEO
DELAY
332
1DA
NOP
JCR(8)
1D8
JCR(7)
1D7
ILR(7)
FF0, K(0)
JCR(6)
15A
DCA(T)
FF0, K(1)
JCR(5)
125
155
NOP
FFC, K(0)
FI (FO)
STC
JFL(3)
f=0
133
JCR(C)
13C
JCC(5)
15C
JCC(6)
16C
JCC(7)
17C
NOP
EFB (H SYNC)
REF → MEM
JCC(9)
19C
JCC(F)
1FC
JCR(6)
END VERTICAL
SCAN DELAY
62
132
ILR(3)
FF1, K(0)
HCZ, FI (MAN)
JFL(7)
f=0
A
COMPLETE
f=1
START FIELD 1
HALF-LINE
173
JFL(8)
182
LTM(A)
K-00, FF0
SDB, DSR
EFA (CLR PAN)
ICR(5)
183
JZR(4)
185
SDR(N)
K(1), FF1
N → F0,3
JCR(6)
104
AC, MDB
JCC(2)
186
NOP
AC, MDB, DCS
JZR(4)
124
ILR(5)
FF0, K(0)
EFB (H CYNC)
FI (TRUE)
REF → MEM
JCR(3)
PRE-VIDEO
DELAY
123
DCA(A)
FF0, K(1)
JFL(2)
f=1
122
ILR(7)
FF0, K(0)
FI (TRUE)
JCR(5)
125
SRA(A)
FF0, K(0)
JFL(4)
f=0*
f=1
143
JCR(5)
145
JCR(6)


JCC(8)
JCC-8
270
1B8
ILR(2)
FF0, K(0)
JCR(C)
1BC
SDR(T)
FF1, K(1)
JCC(C)
BEGIN VERTICAL
RETRACE DELAY
1CC
ILR(5)
FF0, K(0)
FI (TRUE)
JCR(B)
PRE-VIDEO
DELAY
1CB
f=1
DCA(A)
FF0, K(1)
JFL(C)
f=0
1CA
f=1
ILR(7)
FF0, K(0)
JFL(7)
f=0*
VIDEO
DELAY
17B
JCR(6)
176
JCR(8)
178
DCA(A)
FF0, K(1)
JCR(9)
179
f=1
JFL(7)
f=0
17A
ILR(5)
FF0, K(0)
FI (TRUE)
JCR(4)
174
DCA(A)
FF0, K(1)
JFL(9)
f=0*
192
DCA(T)
FF0, K(1)
JCR(9)
f=1
193
DCA(A)
FF0, K(1)
JFL(9)
f=0
f=0
POST-VIDEO
DELAY
199
NOP
REF → MEM
EFB (H SYNC)
JFL(A)
f=1
f=0
1AB
JCR(1)
252
1AA
JCR(F)
1A1
END VERTICAL
SCAN DELAY
1AF
1D8
JCR(7)
1D7
ILR(7)
FF0, K(0)
JCR(6)
1D6
DSM(6)
FF0, K(1)
JCR(9)
1D9
ADR(0)
FF0, K(1)
EFB (H SUNC)
REF → MEM
JFL(B)
f=0
f=1
1BB
NOP
JCR(F)
1BF
JCC(C)
END VIDEO
PORTION
BEGIN VERTICAL
SCAN DELAY
272
1BA
ILR(4)
FF0, K(0)
JCR(6)
1B6
SDR(T)
FF1, K(1)
JCC(F)
1F6
ILR(5)
FF0, K(0)
FI (TRUE)
JCR(B)
1FB
DCA(A)
FF0, K(1)
JFL(F)
PRE-VIDEO
DELAY
f=1
f=0
1FA
ILR(7)
FF0, K(0)
JFL(4)
f=0*
f=1
148
JFL(4)
f=1
143
JCR(5)
145
JCR(6)
146
DCA(A)
FF0, K(1)
JCC(6)
166
JFL(4)
f=1
f=0
VERTICAL SYNC
142
ILR(7)
FF0, K(0)
JCR(4)
START FIELD 2
HALF-LINE
144
SRA(A)
FF0, K(0)
EFA (V SYNC)
JCC(5)
154
NOP
FI (TRUE)
JCR(9)
159
f=0*
JFL(0)
f=1
VIDEO DELAY
10B
JCR(C)
10C
JCR(D)
10D
DCA(A)
FF0, K(0)
JCR(E)
10E
f=0
JFL(0)
f=1
10A
ILR(5)
FF0, K(0)
FI (TRUE)
JCR(3)
POST-VIDEO
DELAY
103



NOTES:

1. ENTRY OF ONLY AC IS A NOP
2. NOP IMPLIES FF0 AND K(0)
3. UNLESS OTHERWISE SPECIFIED, FI CONTROL IS HCZ
4. $R_5 = R_0$
5. R_2, R_4, R_7 EVEN

INITIALIZE:

R_5	PREVIDEO DELAY/POSTVIDEO DELAY ≠0
R_1	INITIAL ADDRESS
R_2	VERTICAL RETRACE DELAY (TOP), ≠, EVEN
R_3	LINES/FIELD
R_4	VERTICAL SCAN DELAY (BOTTOM), = R_2
R_7	WORDS/LINE EVEN

Figure A61. Display.

3

MACROINSTRUCTION SET (TABLE A6 AND A7)

In order to allow any degree of versatility in image processing, the processing system must be programmable; that is, it must be possible to implement any logical sequence of predefined operations with reasonable facility. In addition, these predefined operations must be neither too specific nor too complex, as these either require the invocation of too many operations or restrict the flexibility of the processing. Although the MCU is microprogrammed, a sequence of microinstructions long enough to accomplish any worthwhile task would be extremely difficult to implement. For this reason, a group of predefined operations is implemented in microcode and can be invoked individually by use of the instruction-fetch microroutine previously described. This set of predefined functions is the macroinstruction set and consists of four general groups of instructions: special-purpose image capture and display instructions, a general-purpose arithmetic and logical instruction set which is necessary to perform the various processing transformations of the video data, general-purpose peripheral I/O device data transfer instructions, and special system control.

IMAGE GROUP (GROUP I)

The image instruction group consists of two image capture instructions and one image display instruction. The CAPL (capture line) instruction provides for the capture of a single line of video data and allows specification of the number of pels on the line to be captured and the location in memory at which the data are to be stored. Video data are packed with eight pels in each memory word. The CAPT (capture) instruction is a more general-case capture which allows specification of starting line of a sequence of lines, number of lines, starting pel on each line, and number of pels on each line. The CAPT instruction also stores data in packed form.

The DISP (display) instruction outputs a portion of an image (as stored by a CAPT instruction) for display on a video monitor. DISP provides a 2-to-1 interlace raster-scan display with the appropriate horizontal and vertical sync pulses and proper data formatting if the video field is stored sequentially in main memory. DISP allows specification of lines per field, starting location of image in main memory, pels per line, and horizontal and vertical retrace delays. If the portion of image in main memory was acquired by use of the CAPT instruction, the DISP parameters must correspond to the CAPT parameters for a valid display.

GENERAL-PURPOSE PROGRAM GROUP (GROUP II)

Group II instructions are divided into four classes: memory reference instructions (MRIs), register instructions (RIs), jump or program sequencing instructions (PSIs), and arithmetic and logical instructions (ALIs).

MR class instructions are those which either load from memory or store an accumulator or register value into main memory. MRIs include LDA, STA, STAX, LDX, STX, LSP, and LDK.

TABLE A6. MACROINSTRUCTION SUMMARY.

OPCODE	MNEMONIC	FUNCTION	OPCODE	MNEMONIC	FUNCTION
200	LCA	Load A direct	240	SRO	Shift A right, 1 fill
201	LDAX(x)	Load A indexed	241	SRZ	Shift A right, 0 fill
202	STA	Store A direct	242	SLZ	Shift A left, 0 fill
203	STAX(x)	Store A indexed	243	SRC	Shift A right, circular
204	LDX(x)	Load index register	244	AND	Logical AND (A)
205	STX(x)	Store index register	245	IOR	Logical OR (A)
206	LSP	Load stack pointer	246	XOR	Logical XOR (A)
207	LDK(x)	Load K-register	247	COM	One's Complement (A)
210	CAPT	Capture	250	ADD	Add memory to A
211	CLX(x)	Clear index register	251	SUB	Subtract memory from A
212	INX(x)	Increment index reg	252	INC	Increment A
213	DCX(x)	Decrement index reg	253	DEC	Decrement A
214	DSZ(x)	DCX, skip on 0 result	254	CLA	Clear A
215	DISP	DISPLAY	255	Invalid	
216	HALT	HALT	256	SMC	Set MOS Clock
217	NOP	Null operation	257	Invalid	
220	JP	Jump unconditional	260	MPR	Memory Protect
221	Invalid		261	TRAX(x)	Transfer (A) to index
222	Invalid		262	TRXA(x)	Transfer (index) to A
223	JNN	Jump $A \geqslant 0$	263	PUSH	(A) placed on TOS
224	JPN	Jump $A < 0$	264	POP	(TOS) placed in A
225	JPZ	JUMP $A = 0$	265	LDAC	Load A with constant
226	JNZ	Jump $A \neq 0$	266	ADDC	Add constant to A
227	Invalid		267	SUBC	Subtract constant from A
230	Invalid		270	CAPL	Capture Line
231	JPX(x)	Jump indexed	271	OUTV(x)	Output Video on ch x
232	JPA	Jump A indirect	272		
233	BYT	Shift right 8 bits	273	INPT(x)	Input data block from tape ch x
234	JPI	Jump memory indirect	274	OUTT(x)	Output data block on ch x
235	JPR	Jump subroutine return	275	INP(x)	Input one word on ch x
236	JSR	Jump to subroutine	276	OUT(x)	Output one word on ch x
237*	SKIP	Skip on Skip x set	277	SIOC(x)	Skip on I/O condtn satisfied

(x) indicates modifier sensitive

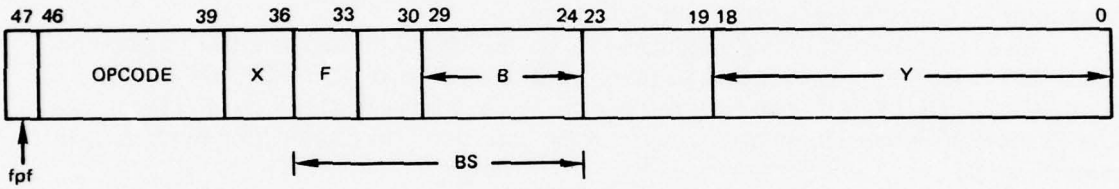
* not yet implemented in hardware

TOS = top of stack

A Accumulator

TABLE A7. MACROINSTRUCTION DESCRIPTIONS.

1) R_6 and R_7 contents are altered during the course of certain instructions. Some block transfer instructions require prior register setup (R_2, R_5, R_1, R_6).
2) Before executing, a program stack pointer (R_8) should be set to desired first stack location.
3) All arithmetic and logical instructions leave the result in the accumulator.
4) Interrupt sequence assumes handling routine to be resident at location 0 in program storage.
5) Memory protect is program-accessible only in that it protects those portions of memory designated by front-panel switches on invocation of MPR instruction. Unless this effect is required, MPR should be used only from front panel. Memory protect does not protect against loss of refresh or loss of power.
6) Any interrupt service routine must end with JPR to restore to entry conditions. If any registers are used, they must be saved in temporary locations before execution of the ISR and the values returned after execution.
7) Subroutine jump destroys contents of R_7 : R_7 used in lowest-level routine or save before JSR.



fpf	=	front-panel fetch	B	=	byte select
X	=	index modifier	Y	=	address or constant
F	=	function code modifier	BS	=	block size
( )	=	contents of	A	=	accumulator
→	=	replaces contents of	AT	=	accumulator or T register
R_x	=	index register X	K_x	=	K register X
S	=	stack pointer (R_8)	P	=	program counter (R_q)
SK_x	=	skip button x	i	=	bit i of register

R class instructions are those which directly affect the contents of one of the index/counter registers in the MCU central processor. RIs include CLX, INX, DCX, DSZ, and TRAX.

PS class instructions control the program flow by either unconditional or conditional program branch. This includes unconditional jump (JP), conditional jumps (JNN, JPN, JPZ, JNZ) indirect jumps (JPI, JPA), and subroutine jump and return (JSR, JPR).

AL class instructions directly affect the contents of the accumulator and include arithmetic instructions (ADD, SUB, INC, DEC, ADDC, SUBC), logical instructions (SRO, SRZ, SLZ, SRC, AND, IOR, XOR, COM, BYT), and the accumulator initialization instructions (CLA, LDAC, PUSH, POP).

I/O GROUP (GROUP III)

Group III consists of both byte transfer and block transfer instructions as well as an I/O condition test instruction (SIOC). Byte transfer instructions are simple single-byte transfers with no condition checks. Proper conditions for input (INP) and output (OUT) of single bytes must be tested for by use of the SIOC instructions.

Two block-transfer output instructions allow high-speed transfer of either program or ASCII data as six 8-bit bytes for each memory word (OUTT) or as eight 8-bit pels for each memory word (OUTV) with two leading 0's added to the 6-bit pels. Block transfer input (INPT) allows high-speed input of 8-bit bytes to be packed into memory with 6 bytes in each memory word.

SYSTEM CONTROL GROUP (GROUP IV)

Group IV consists of those instructions which allow the MCU user to explicitly specify hardware operations. Group IV instructions include: HALT (which stops the system clock at the beginning of the next instruction-fetch cycle), SMC (which toggles the clock between MOS and HS to allow use of both micromemories under program control), and MPR (which sets the memory protect feature).

Two other functions, which are not normally used as program instructions but do exercise system control, are INTERRUPT and BOOTSTRAP. Each of these "instructions" is invoked by a hardware signal sequence.

$OPCODE_8$	MNEMONIC	FUNCTION	DESCRIPTION
200	LDA	$(Y) \rightarrow A$	Load accumulator (acc)
201	LDAX(x)	$(Y + R_X)$	Load acc with contents of memory location $R_X + Y$
202	STA	$A \rightarrow Y$	Store contents of acc in memory location Y
203	STAX(x)	$A \rightarrow Y + R_X$	Store contents of acc in memory location $Y + R_X$
204	LDX(x)	$(Y) \rightarrow R_X$	Load index R_X with contents of memory location Y
205	STX(x)	$R_X \rightarrow Y$	Store contents of R_X in memory location Y
206	LSP	$(Y) \rightarrow S$	Load stack pointer with stack start location
207	LDK(x)	$(Y) \rightarrow K_X$	Load K_X with contents of memory location Y
210	CAPT		Initiate capture routine in TTL ROMs
211	CLX(x)	$0 \rightarrow R_X$	Clear index R_X
212	INX(x)	$R_X + 1 \rightarrow R_X$	Add 1 to contents of R_X
213	DCX(x)	$R_X - 1 \rightarrow R_X$	Subtract 1 from contents of R_X
214	DSZ(x)	$R_X - 1 \rightarrow R_X$ If result = 0: $P + 1 \rightarrow P$	Subtract 1 from contents of R_X skip the following instruction
215	DISP		Initiate the DISPLAY routine in TTL ROMs
216	HALT		Sets STEP MACRO and stops MCU clock
217	NOP		No operation
220	JP	$Y \rightarrow P$	Transfer program control to memory location Y
221		Not used	
222		Not used	
223	JNN	if $A \geqslant 0$	If contents of acc are not negative ($\geqslant 0$), then jump to Y
224	JPN	if $a < 0$ $Y \rightarrow P$	If contents of acc are negative (< 0), then jump to Y
225	JPZ	if $A = 0$ $Y \rightarrow P$	If contents of acc are zero, then jump to Y
226	JNZ	If $a \neq 0$ $Y \rightarrow P$	If contents of acc are not zero, then jump to Y
227		Not used	
230		Not used	
231	JPX(x)	$R_X + Y \rightarrow P$ $Y \rightarrow P$	Jump to location specified by sum of the contents of R_X and Y
232	JPA	$A \rightarrow P$	Jump to location specified by the contents of acc

$OPCODE_8$	MNEMONIC	FUNCTION	DESCRIPTION
233	BYT	$A_i \rightarrow A_{i-8} \pmod{47}$	Rotate acc right 8 bits
234	JPI	$(Y) \rightarrow P$	Jump to location specified by the contents of Y
235	JPR	$((S)) \rightarrow P$ $S - 1 \rightarrow S$	Jump to location specified by the top stack element
236	JSR	$P \rightarrow (S)$ $S + 1 \rightarrow S$ $Y \rightarrow P$	Store contents of program counter on top of stack Jump to Y
*237	SKIP	if SK_x $P + 1 \rightarrow P$	If $SKIP_x$ has been set, then skip the following instr
240	SRO	$A \rightarrow A_i - Y$ $1 \rightarrow A_{47} - A_{47} - Y$	Shift contents of acc right Y bits and fill left end of acc with 1's
241	SRZ	$A_i \rightarrow A_i - Y$ $0 \rightarrow A_{47} - A_{47} - Y$	Shift contents of acc right Y bits and fill left end of acc with 0's
242	SLZ	$A_i \rightarrow A_i + Y$ $0 \rightarrow A_0 - A_{Y-1}$	Shift contents of acc left Y bits and fill right end of acc with 0's
243	SRC	$A_i \rightarrow A_i - Y \pmod{47}$	Shift contents of acc right Y bits shifted off right end and fill left end of acc with the Y bits shifted off right end
244	AND	$A \wedge (Y) \rightarrow A$	Logically AND the contents of memory location Y with contents of the acc
245	IOR	$A \vee (Y) \rightarrow A$	Logically Inclusive OR the contents of memory location Y with contents of the acc
246	XOR	$A + (Y) \rightarrow A$	Logically Exclusive OR the contents of memory location Y with contents of the acc
247	COM	$A \rightarrow A$	Logically (1's) complement the contents of the acc
250	ADD	$A + (Y) \rightarrow A$	Add the contents of memory location Y to the contents of the acc
251	SUB	$A - (Y) \rightarrow A$	Subtract the contents of memory location Y from the contents of the acc, leaving a 2's complement result
252	INC	$A + 1 \rightarrow A$	Add 1 to the contents of the acc
253	DEC	$A - 1 \rightarrow A$	Subtract 1 from the contents of the acc
254	CLA	$0 \rightarrow A$	Set the contents of the acc to zero
255		Not used	
256	SMC		Set MOS clock
257		Not used	

$OPCODE_8$	MNEMONIC	FUNCTION	DESCRIPTION
260	MPR (Y)	$Y \rightarrow$ MP Register	Enable memory protect for the 4k blocks of memory for which those bits in Y are set. Y is from front-panel bits 18 to 0
261	TRAX(x)	$A \rightarrow R_x$	Contents of acc are copied into index register
262	TRXA(x)	$R_x \rightarrow A$	Contents of index register are copied into acc
263	PUSH	$A \rightarrow (S)$ $S + 1 \rightarrow S$	Contents of acc are copied onto top of stack and stack pointer is incremented
264	POP	$((S)) \rightarrow A$ $S - 1 \rightarrow S$	Contents of top of stack are copied into acc and stack pointer is decremented
265	LDAC	$Y \rightarrow A$	Load Y into acc
266	ADDC	$A + Y \rightarrow A$	Add Y to acc
267	SUBC	$A - Y \rightarrow A$	Subtract Y from acc
270	CAPL	Capture line	Capture one line from the video scanner for the number of words specified by the contents of R_7 and store at address specified by Y. R_2 must be previously set to $R_2 = 7$ R_7 = number of words - 1
271	OUTV(x)	Output video	Place one video record on tape channel x. Data begin at location Y in memory and continue for the number of words specified by the contents of R_6. Requires the constant 7 to be in R_2 and 77 to be in K_3
272		Not used	
273	INPT(x)	Read tape buffer	Transfer a data block from channel x to a buffer beginning at location specified by the contents of R_6
274	OUTT(x)	Write tape buffer	Transfer to channel x the contents of a buffer beginning at location Y and ending at location Y + BS
275	INP(x)	$(I/O\ ch)_x \rightarrow Y$	Input one word on I/O channel x to memory location Y
276	OUT(x)	$(Y) \rightarrow I/O\ ch_x$	Output one word from memory location Y on I/O channel x
277	SIOC(x)	Skip on I/O condition	If I/O condition x is satisfied, then skip next instruction

I/O channels:

x	device
0	none
1	none
2	Versatec printer/plotter
3	none
4	none
5	RS232, 9600 baud
6	Magnetic tape unit
7	IEEE 488 GPIB which includes Tektronix 4051 graphic system Digital Image Analyzer Hardware Illumination Corrector

SIOC functions

xf	function
00	none (skip always)
10	TERMINAL DATA READY
20	TERMINAL BUSY
30	File Mark
40	Scanner Data Available
50	ACDS (accept data state)
60	LACS (Listener active state)
70	t_x gate
01	t_x data
11	RSV (request for service)
21	EOI (end or identify)

The following instructions are not normally recognized as opcodes but may be used as such.

OPCODE	FUNCTIONS	COMMENTS
006	EXAMINE	(FP) → R_7; ((R_7)) → Display
007	EXAMINE NEXT	R_7 + 1 → R_7; (R_7)) → Display
017	FETCH	(equivalent to NOP)
030	DEPOSIT	(FP)* → (R_7): Examine Next
135	SET AC	(FP) → A
137	SET R_n	(FP) → R_n**
175	DISPLAY AC	(A) → Display
177	DISPLAY R_n	(R_n)** → Display
000	FAULT	
363	BOOT	
362	INTERRUPT	

* FP = front-panel data switches

** n is 10-position lever switch; accumulator value is lost when used in this mode

OPERATION

The MCU can currently be operated either from its own front panel or in an interactive environment with a Tektronix 4051 Graphic System. The MCU can always be operated from the front panel but can only be operated from the 4051 after the appropriate software has been loaded into program memory. Generally, the front panel is used only for debugging software and hardware, but it may also be used to enter and edit programs.

PROGRAM ENTRY AND EDITING

Programs may be entered and edited via the front panel by using the EXAMINE and DEPOSIT instructions. The memory location at which the program is to reside is set in the low-order 16 bits of the front-panel switch register, and the EXAMINE opcode (006_8) in the high-order 9 bits. The front-panel-fetch (fpf) bit is set to 1 and STEP MACRO is pressed. The front-panel octal displays will then show the current contents of the specified memory location. If the contents are as required, the EXAMINE NEXT opcode (007_8) is set and STEP MACRO pressed, displaying the contents of the next memory location. If the examined contents are not as required, the proper data are set in the switch register and DEPOSIT is pressed, which causes the switch register contents to be placed in the currently examined location and the contents of the next location to be displayed. At this time, one of four operations can be performed: (1) set a new value in the switch register and DEPOSIT as before, (2) set EXAMINE NEXT opcode and fpf bit and STEP MACRO to examine the next location, (3) set EXAMINE opcode and fpf bit as well as a new address and STEP MACRO to examine a different area of memory, or (4) discontinue the EXAMINE/DEPOSIT sequence.

This process is quite tedious, and program entry and editing are accomplished much more easily by use of the interactive MONITOR. This method is therefore reserved primarily for modification of individual memory locations during program execution.

MODE CONTROL BUTTONS

In order to provide for manual control of program execution, four mode control buttons are provided on the front panel. Two step controls, a repeat function, and a run button provide an operator with versatile control of program execution. Testing and debugging can be done at the macrolevel or at the microlevel. In the instruction hierarchy, macroinstructions fetched from memory by use of the program counter (R_9) are implemented as sequences of microinstructions. In normal operation the contents of R_9 are used by the fetch sequence as an address for a memory read operation. The data fetched from memory become the macroinstruction to be executed. The high-order bits of the data from memory (the opcode) are loaded into the micromemory address sequencer at the end of the fetch operation. The macroinstruction is then executed in the microcode with the last microinstruction returning microlevel control to the fetch sequence. The program counter (R_9) is incremented in order to fetch the next instruction or is loaded by a jump, branch, or skip instruction.

The two step buttons are used for program testing and debugging at either the macrolevel or the microlevel. If STEP MICRO is selected, each touch of the STEP MICRO button will pass one system clock pulse, which allows the execution of a single microinstruction. In this way microroutines may be executed one step at a time. The STEP MACRO button enables one complete fetch/execute cycle. Therefore, typical machine language programs may be executed one step at a time for macroprogram debugging purposes. Incorporated into the microcode is a display of the accumulator contents whenever they are modified and the STEP MACRO mode button is active. This is designed as an aid to simplify debugging operations. The REPEAT button is used in conjunction with either step button or the RUN button as a further aid to microlevel or macrolevel testing. If STEP MICRO and REPEAT are selected simultaneously, the clock pulse to the 3001 microcontrol unit will be inhibited. Each time the STEP MICRO button is touched, therefore, the same microinstruction will be executed. The entire system performs normally, with the exception of the 3001 microcontrol unit. Similarly, if REPEAT and STEP MACRO are selected, the increment of the program counter (R_g) will be inhibited. The same microroutine will be fetched and executed each time the STEP MACRO button is touched. Since these step functions occur on a single-shot basis, they are not observable by test equipment requiring repetitive waveforms. The RUN button may be used in conjunction with the step/repeat functions in the following manner. If either step/repeat function has been selected and the RUN button is touched, the system will repetitively execute a single microinstruction or a single macroinstruction. Test equipment such as oscilloscopes, waveform monitors, counters, and logic analyzers may then be used to verify proper system operation at the signal level.

INTERACTIVE OPERATIONS

Because the entire macroinstruction set is available and instructions may be executed one at a time from the front panel, the MCU may be operated entirely from the front panel. As mentioned, however, this mode of operation is quite tedious and extremely time-consuming. For this reason, a software system MONITOR has been developed in order to allow the MCU users to operate the entire system using high-level English-oriented commands. The following is a description of the operation of the MCU MONITOR.

System power-up is designed to be very simple, accomplished primarily by pressing a few buttons, First, insert the 4051 Terminal Executive magnetic tape cartridge into the 4051 tape drive and press AUTOLOAD. When a message is displayed on the 4051 screen, press user-definable key (UDK) 1. The 4051 software monitor is now active. Next, position the Kennedy tape units at load point with a program tape on unit 1, set MCU front-panel switches to all 0's and press BOOTSTRAP. When the tapes stop, the memory controller software MONITOR is active. These operations cause the first logical file on each tape to be loaded into program memories (4051 and MCU, respectively) and interactive operation to commence.

The MCU and the 4051 are each capable of executing programs completely independently. The 4051 is a self-contained system including I/O, but the MCU has no self-contained high-level input capability. For this reason, the two devices are programmed and connected in an interactive environment. As a result, the 4051 can be used to issue commands to the MCU following which each device may execute its own programs, which may be completely unrelated and may take seconds, minutes, or hours to complete. The primary reason for this organization is that system users may enter high-level English-oriented commands rather than a complex sequence of machine-level commands.

Features of this system include an "operation complete" response to the user, extensive error test and recovery both for equipment error and operator error, peripheral device commands which simplify such operations as saving programs and tables on magnetic tape and retrieving them from tape, and interrupt capability which allows an external device to signal the control system that some operation is required by the device.

An important function of the MONITOR, which is not a command in itself but which makes use of MONITOR commands, is Inspect and Change. This function is a keyboard equivalent of the front-panel program entry and editing operations. Table A8 is a list of the major MONITOR commands.

TABLE A8. MCU MONITOR COMMAND SUMMARY.

RETURN	Retrieves the value of a specified memory location for display on the 4051
STORE	Saves a specified data value in a specified memory location
GOTO	Causes program execution in the MCU to switch from MONITOR to a special-purpose program. When execution is complete, the program must return control to MONITOR.
WRITE	Places on magnetic tape a single logical record consisting of the data occupying a specified block of memory locations
READ	Places in a specified location of memory the contents of a single logical record off magnetic tape
REWIND POSITION SBK SFK BBK BFK	A combination of these instructions positions magnetic tape unit at any desired location (file and record)
FILEMARK	Places a filemark on magnetic tape
MOVE	Transfers a block of data from one set of memory locations to another
DISPLAY	Displays a specified 440-line by 432-pel segment of an image from tape on a video monitor
SEARCH	Allows selective examination and modification of a block of memory based on a specified bit pattern

RESULTS

The Image Capture and Analysis System (ICAS) is presently undergoing a major upgrading process. The actual demonstration of the new performance goals cannot be made until all modifications are incorporated and debugged. Insofar as possible, all modifications to the ICAS will be accomplished in a manner and a time sequence such as to minimize system downtime. There will be changeover periods throughout the upgrade during which the equipment will be inoperable. The results of the system upgrade can best be defined by comparing the specifications of the FY76 and FY77 configurations (table A9).

TABLE A9. ICAS SPECIFICATIONS.

Large Drum Test Bed	FY76 Configuration	FY77 Configuration
Line scan rate	To 10.5 Mpels/s (Fairchild CCD110)	To 84 Mpels/s (RCA TDI TC1212 imager)
Copy scan rate	2.5, 5, 10, 20 each 8½-by- 11-inch pages/s	To 20 each 8½-by-11-inch pages/s
A/D conversion rate	To 10.5 Mpels/s (Datel ADC UH6B)	To 84 Mpels/s (Phoenix Data 1106-60 and 1106-100)
A/D conversion resolution	One part in 64 (6 bits) linear	One part in 64 (6 bits) linear
Sample & hold acquisition	50 ns (Datel SHM-UH)	5 ns (Phoenix Data converters)
Illumination source	Quartz-iodide to 1500 watts	Two fluorescent tubes @ 33 watts each
D/A conversion rate	To 85 Mpels/s @ 9 bits plus sign (Motorola GFE)	To 85 Mpels/s @ 9 bits plus sign (Motorola GFE)
Digital Image Analyzer		
Input data rate	To 22 Mpels/s max	To 22 Mpels/s max
Input capacity to memory	To 16.77×10^6 (2^{24}) identical inputs	To 16.77×10^6 (2^{24}) identical inputs
Dynamic range	To 64 different input grey levels	To 64 different input grey levels
Output rate from memory	To 22 Mbits/s max	To 22 Mbits/s max
Memory Control Unit and Display		
Memory capacity	3.145×10^6 bits (65 536 words at 48 bits)	25.16×10^6 bits (65 536 words at 384 bits or 522 288 words at 48 bits)
Video input/output byte	Six bits	Six bits
Video input/output rate	To 11 Mbytes/s max	To 11 Mbytes/s max
Display vertical frequency	15 to 60 fields/s (Conrac RQB17/C)	15 to 60 fields/s (Conrac RQB17/C)
Display horizontal frequency	15 to 40 kHz (Conrac RQB17/C)	15 to 40 kHz (Conrac RQB17/C)
Video input voltage	0.3 to 3.0 V peak-to-peak (Conrac RQB17/C)	0.3 to 3.0 V peak-to-peak (Conrac RQB17/C)
Video input impedance	50k ohms shunted by 10 pF (Conrac RQB17/C)	50k ohms shunted by 10 pF (Conrac RQB 17/C)
Video frequency response	±1 dB @ 30 MHz, ±6 dB @40 MHz (Conrac RQB17/C)	±1 dB @ 30 MHz, ± 6 dB @ 40 MHz (Conrac RQB17/C)
Display size	14 inches wide by 11 inches high (Conrac RQB17/C)	14 inches wide by 11 inches high (Conrac RQB17/C)
Image memory rack dimensions	21½ inches wide by 26 inches deep by 70 inches high	21½ inches wide by 26 inches deep by 70 inches high

CONCLUSIONS

1. The upgraded ICAS will provide the capability for many tests not possible with the FY76 configuration as shown in table A10.

2. The new capabilities will include:

a. Capture of a full page of data at a 20-page-per-second rate.

b. Operation in the time-delay integration (TDI) mode with a four-channel imager.

c. High-speed operations on data in the full-page Frame-Store Memory.

d. High-speed transfers of data between the Frame-Store Memory and Tapes.

e. With a properly designed personality module, operation at 84 megapels per second from a single sensor source.

TABLE A10. ICAS TYPICAL TEST ACCOMMODATED.

Scanner Tests

- Illumination requirements
- Dynamic range
- Signal quality vs shift rate
- Signal quality vs clock noise
- Abutment problem approaches
- Signal quality vs copy velocity
- Signal quality vs illumination color
- Resolution requirement subjective evaluation
- Time delay integration tests

Image Analyzer Tests

- Threshold detection studies
- Dynamic range analysis
- Dynamic range vs illumination color
- Run length compression studies

Analog-to-Digital Converter Tests

- Preamp level control
- Preamp gain control
- Sample-and-hold circuit studies
- A/D signal-to-noise vs speed
- Grey scale reduction effects
- Nonlinear converter studies

Frame-Store Memory and Display Tests

- Edge enhancement techniques
- Acquisition rate evaluation
- Image data reconfiguration studies
- Line rate/frame rate studies
- Interlace vs noninterlace studies
- Evaluate appropriate compression algorithms
- Evaluate appropriate enhancement algorithms

APPENDIX B:
IMAGE RESOLUTION

Prepared for

US POSTAL SERVICE
July 1977

by

SIGNAL ANALYSIS AND IMAGE PROCESSING BRANCH
(Code 7323)

NAVAL OCEAN SYSTEMS CENTER
San Diego, CA

CONTENTS

ILLUSTRATIONS

TABLES

INTRODUCTION

In March 1977 the USPS Design Division was invited to participate in an investigation of imaging resolution parameters for the Electronic Message Service System (EMSS) by the RCA, Camden, EMSS Program Office. After studying the requirements, it was determined that the NOSC Image Capture and Analysis System (ICAS) could be readily upgraded to perform the image acquisitions required.

Since the experiment required significant manpower, NOSC was allowed to substitute this data acquisition and a descriptive report for the advanced image enhancement work which would otherwise have been undertaken during this period.

At the time of this writing, most of the hard-copy prints to be made from the tape data have not been completed. Considerable data are now available covering the preparation of the test bed, the actual acquisition of the images, and the correction and formatting of the results. These portions of the task will be reported at this time. The images and a discussion of the results will be published as soon as the actual images are available.

SPECIFIC TEST OBJECTIVE

The specific objective of this study was to provide the high-quality digitized images to RCA, Camden, in support of one of the RCA EMSS tasks which pertains to the determination of resolutions which should be specified when the graphic scan mode of the system is used.

RCA cites the rationale for the tests. This is quoted as follows: "There are three major reasons for this. First, a major aspect of the RCA task is to tap the subjective judgement of realistic potential users, and requires that full-page document samples be available for evaluation in order to provide a realistic overall impression to the judge. Second, it is important to simulate a wider range of resolution values, and with closer-spaced steps, than available from other work. A third consideration is that the scanning and reproducing mechanisms should be known, controlled, and as representative of actual potential EMS processes as possible."

IMAGES TO BE SCANNED

A set of nine master documents sent to NOSC was to provide the subjects for the tests. These are included here as figures B1 through B9. RCA feels that this set contains the range of types of information which may be typical of the bilevel (black and white) images to be transmitted. They include typed, handwritten, and graphic images. The designators assigned to the samples are as tabulated below.

Figure	Designator	Descriptor
B1	A-1	FLASH FLASH FLASH $
B2	A-2	FOUR NEWSPAPER ADS
B3	C-1	LETTER FROM SANYO TO ELECT
B4	C-2	RCA LETTER FROM REGAN TO HAYNES
B5	C-3	HANDWRITTEN LETTER
B6	T-1	D.C. HEATH & CO.
B7	T-2	RCA FORM
B8	T-3	NEW HAMPSHIRE BALL BEARING
B9	S	FINE TYPE, GRAPHICS, ETC

RESOLUTIONS TO BE CAPTURED

The scan densities (resolutions) requested by RCA ranged from 120 by 120 pels per inch to 600 by 600 pels per inch in a ratio of increasing scan densities approximating $\sqrt[5]{3}$ steps. The closest convenient values from the standpoint of accuracy control turned out to be 120, 160, 200, 240, 300, 400, 480, and 600 pels per inch in both dimensions. All images were captured by allowing 6 bits per pel for the 64 possible brightness levels.

FLASH! FLASH! FLASH!

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$$$$$$$$ $$$$$$$$

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Sunday, January 26, 1975 - 10 AM to 5 PM
Monday, January 27, 1975 - 9 AM to 8 PM

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You can save money on many of the finest names in Nationally Advertised Furniture, displayed in a magnificent 160,000 sq. ft. showroom.

Don't pass up this special Two Day offer, closed to the public, but opened to members of United Buying Service.

A Purchase Certificate is necessary to gain admittance to our FABULOUR FURNITURE SALE on Sunday, Jan 26 from 10 AM to 5 PM, or on Monday, Jan. 27 from 9 AM to 8 PM.

CONTACT OUR OFFICE TODAY - TREMENDOUS *SAVINGS CAN BE YOURS!!*

Figure B1. Sample A-1.

Figure B2. Sample A-2.

SANYO

SR-75-059

SANYO ELECTRIC INC.
51 JOSEPH STREET
MOONACHIE, N.J. 07074
Phone (201)641-2333

March 14, 1975

RCA
Advanced Technology Laboratories
Camden, New Jersey

Dear Sir:

I am very much interested in your Non-Impact Technical Line Printer.

If possible, please send me this information or literature at your earliest convenience.

Thank you.

Very truly yours,

SANYO ELECTRIC INC.

O. Suzuki
Engineering Representative

Figure B3. Sample C-1.

Mr. H. E. Haynes
RCA Corporation
Marne Highway
Moorestown, New Jersey 08057

RCA

Dear Harold: May 28, 1974

I am enclosing a photograph showing your award presentation at the March Inventors Recognition Dinner which I thought you might be pleased to have.

I was delighted that you were able to attend this affair and I hope that any future affair will be as enjoyable.

Best regards,

J. V. Regan

Enc

Figure B4. Sample C-2.

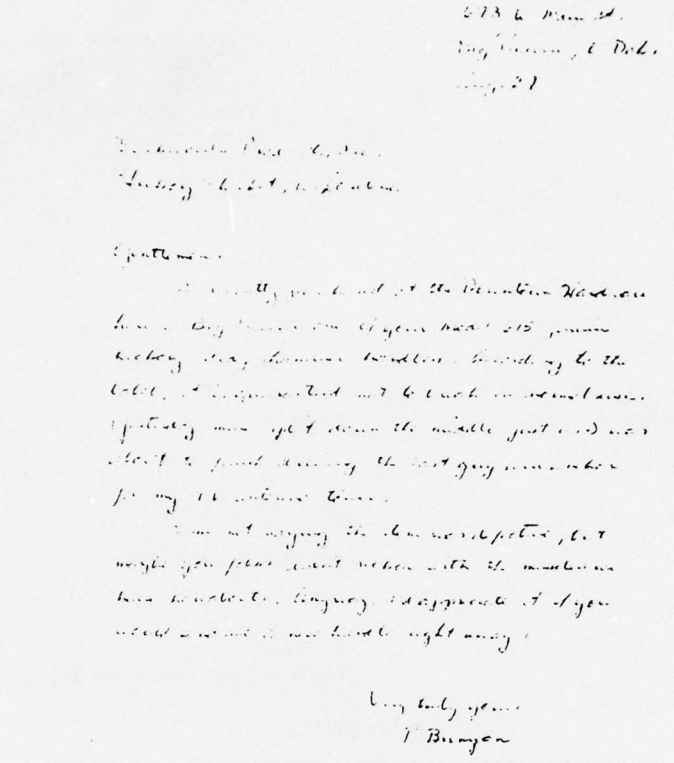

Figure B5. Sample C-3.

DATE
03-06-5

INVOICE: 510461-0
ACC: 1151845
SHIP 1-161843

FROM: D.C. HEATH & CO

TO: Boyell, Roger L.
Govt. & Comm. Systems
RCA Corp.
Moorestown, N.J.

Bestway Prepaid

Quant. Ordered	Quant. Shipped	Cat. No.	Item	Unit Price	Amount
1	1	095935	Sonar & Underwater Sound	13.00	13.00
			Subtotal		13.00
			Transportation & Handling		.66
			Sales Tax		.65
					14.31

Remit to D.C. Heath & co.
P.O. Box 3191
Boston, Mass. 02241

Figure B6. Sample T-1.

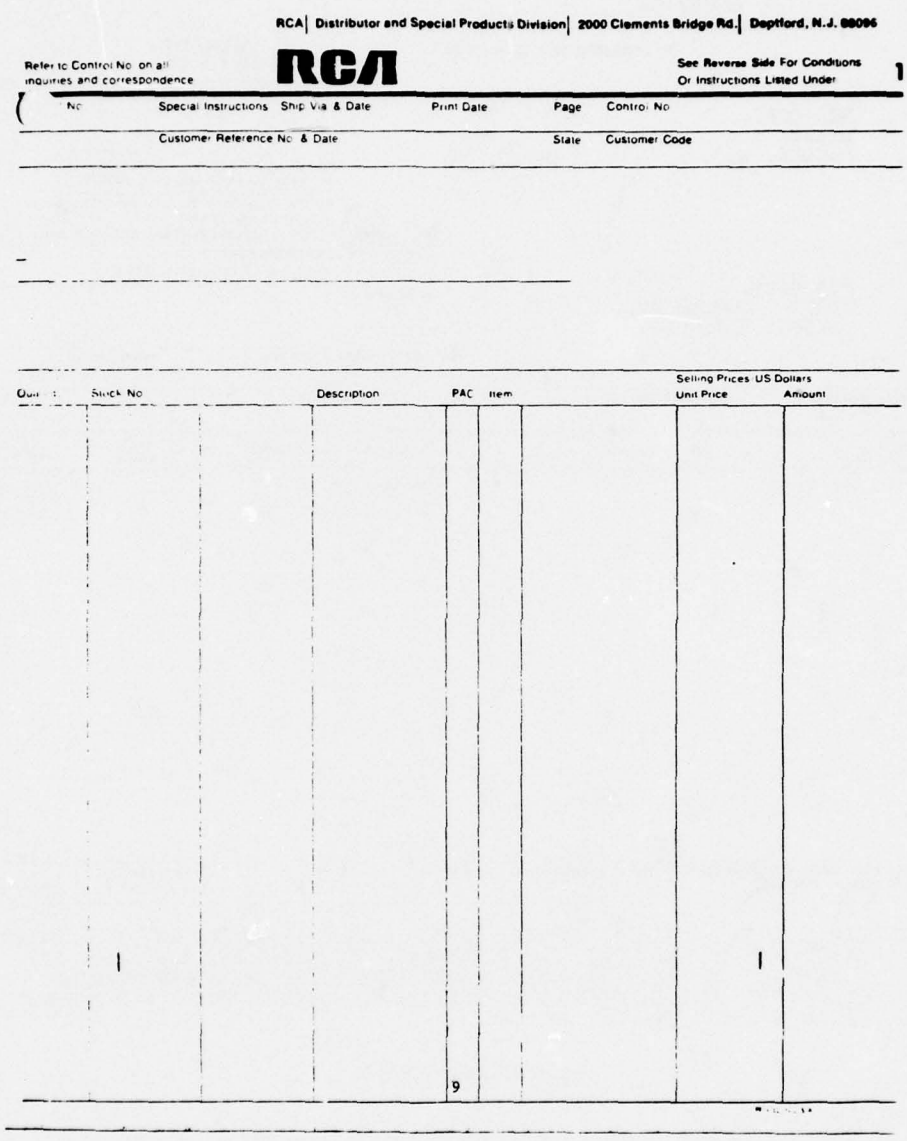

Figure B7. Sample T-2.

NEW HAMPSHIRE BALL BEARINGS, INC.
PETERBOROUGH, N. H. 03458

INVOICE

INVOICE DATE	INVOICE NUMBER	PAGE NO
02/20/76	02-8000	1

PLEASE REFER TO THIS NUMBER ON ALL INQUIRES AND CORRESPONDENCE

RETURN ONE COPY OF THIS INVOICE WITH YOUR REMITTANCE

REMIT TO U.S. ROUTE 202 PETERBOROUGH, N.H. 03458

SHIP TO
RCA CORP.
DELAWARE & MARKET ST.
CAMDEN, N.J. 08102

BILL TO
RCA CORP.
FRONT & COOPER STS.
CAMDEN, N.J.

CUST NO	CUSTOMER ORDER NO.	R
18080	08615 3504-11-C15	G

NMBB ORD

DATE SHIPPED	SHIP VIA	WAYBILL NO

TERMS

ORDER DATE	INSPECTION	CERTIFICATION	CONTRACT NUMBER	PC
				A

ITEM NO	QUANTITY SHIPPED	ITEM DESCRIPTION	CUSTOMER PART NUMBER	UNIT VALUE	TOTAL
1A	--	MISC.	DEP 30607	--	116.80
1B			DEP 30653		34.18

THESE GOODS WERE MADE IN COMPLIANCE WITH THE FAIR LABOR STANDARDS ACT OF 1938 AS AMENDED

PARTIAL

FINAL F

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NOTES

SPECIAL INVOICE COVERING DEDUCTIONS TAKEN ON 8/14/75 FOR INVOICES DATED IN MARCH 1975 ON DEP 30607 AND DEP 30653. TO DATE, BEARINGS HAVE NOT BEEN RETURNED TO N.H.B.B. THESE DEDUCTIONS COVER PARTS RECEIVED AND RESHIPPED BY N.H.B.B. AT NO CHARGE AFTER CORRECTIVE ACTION WAS TAKEN. SEE ATTACHED MATERIAL FOR DETAILS.

Figure B8. Sample T-3.

Figure B-9. Sample S.

ICAS PREPARATIONS

There were two areas within the ICAS which required upgrading in order to accommodate the variable resolution tests. RCA originally requested scan densities of 120, 160, 200, 250, 320, 390, 490, and 600 and recommended a tolerance limit of ±3% on these values. It was later determined that the scan density values were somewhat flexible, but the tolerance was felt to be important. It was therefore necessary to instrument the ICAS to ensure that the tolerance could be consistently verified during the tests. The accuracy of scan in the direction of copy motion is a function of the relationship of the Baldwin angular encoder output to the actual incremental motion of the copy. Therefore, modifications to the test bed needed consideration. The accuracy of scan across the documents is a function of lens parameters and object-to-image distance. Therefore, considerations of a test target and software calibration procedure were required.

LARGE DRUM TEST BED PREPARATIONS

The greatest concern involving the Large Drum Test Bed (LDTB) modifications was related to improving the resolution of the Baldwin encoder with respect to the incremental copy motion. Also, the actual speed of the drum required careful control in order to obtain the maximum safe acquisition speed without exceeding the allowable rate of transfer of data to the Kennedy tape deck. It was felt that sufficient illumination was available for the tests, but considerations would be required to ensure consistency of integration time and minimization of smear at the lower resolutions.

EXISTING DRUM DESIGN

The source of the incremental marks representing the 0.005-inch advancement of the copy on the 40.96-inch-circumference drum was the positive-going edge of one of the two quadrature square wave outputs from the Baldwin encoder. Since this provided only 200 pels per inch and a combination of all four rising and falling edges of both tracks only produced 800 pels per inch with no convenient way of producing even spacing at 600 pels per inch and some of the other desired values, it was decided to try the relative rotation of the main scanning drum and the Baldwin encoder by using a pair of pulleys and a neoprene belt.

The LDTB was configured as shown in figure B10. The small, low-speed synchronous drive motor, which rotates at 0.5 rev/min, was belt-driven directly to the main scanning drum shaft. If further reduction in drum speed was required for the higher-resolution tests, the power train included an idler and pair of speed-reducing pulleys. The ratio of angular movement of the main scanning drum and the Baldwin encoder could be chosen by selecting various ratios of pulley diameters.

The nominal motion ratio was very good at all values. Experimentation showed that with 0.1875-inch neoprene belt material very accurate ratios can be predicted by turning the diameter of the bottom of the V-groove 0.137 inch less than the calculated diameter.

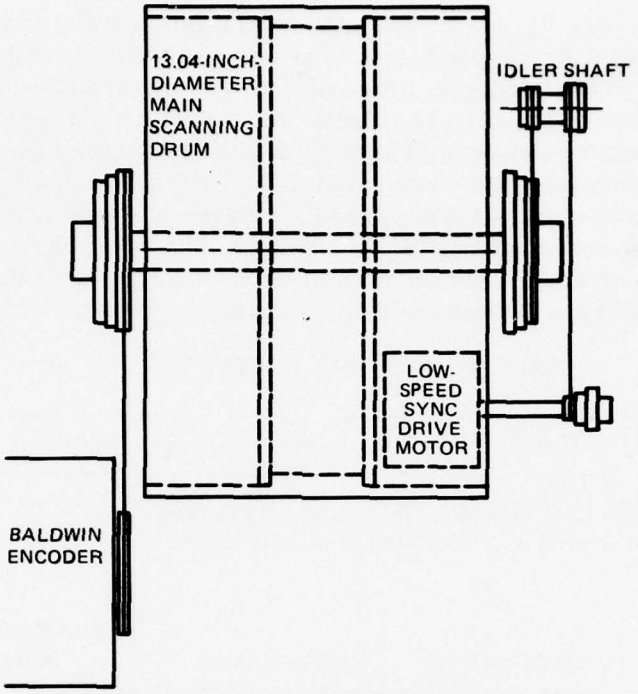


Figure B10. Variable resolution with existing drum design.

The parts were then fabricated, mounted, and tested. The values of instantaneous velocity of the encoder were extremely nonuniform. In some instances the variation was as much as 100 to 1 when the interval between encoder outputs was displayed on an oscilloscope.

It was felt that the motion of the high-inertia drum was much more uniform, but there was no way to instrument a verification test. In addition, the command to scan a line was made directly from the encoder outputs, which would lead to nonuniform spacing in the line acquisitions.

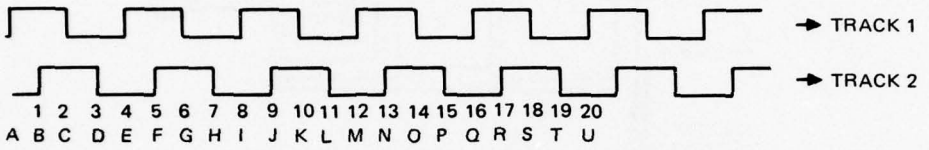
An attempt was made to reduce the "stiction" in the encoder bearing. The bearings were removed, cleaned, and reassembled. This improved performance of the equipment but not enough to justify the approach. The manufacturer stated that the bearings used were class 7 (as were the bearings used on the main scanner drum shaft). The encoder bearings are highly loaded and cannot be relieved without degrading the performance. Since the approach was considered unworkable, it was dropped in favor of the alternative described in the following section.

NEW DRUM DESIGN

A strategy exploiting the use of smaller drum diameter and returning the Baldwin encoder to the main shaft was investigated. The small drum test bed (SDTB) has a drum which is 12 inches in circumference. This candidate diameter of 3.820 inches and two others were considered. The other two choices were two-thirds and one-third of the diameter of the main scanner drum. The SDTB drum was eliminated from the choices because the 12-inch circumference when divided into 8192 increments would yield multiples of 0.001464-inch steps, which would lead to odd values of scan densities acquired.

Table B1 shows the relationships of resolution values available for the main scanner drum and the two others. The main scanner drum was eliminated immediately because a scan density of 600 pels per inch could not be acquired with such a drum.

TABLE B1. BALDWIN ENCODER OUTPUTS.



Std Drum 13.03797-in Dia	8.69189-in Drum	4.34599-in Drum	RCA Requested Values	$\sqrt[5]{3}$ Ratios
A → B = 800	A → B = 1200	A → B = 2400		
A → C = 400	A → C = 600	A → C = 1200		
A → D = 266.7	A → D = 400	A → D = 800		
A → E = 200	A → E = 300	A → E = 600	600	600
A → F = 160	A → F = 240	A → F = 480	490	481.6
A → G = 133.3	A → G = 200	A → G = 400	390	386
A → H = 114.286	A → H = 171.429	A → H = 342.858		
A → I = 100	A → I = 150	A → I = 300	320	310
	A → J = 133.33	A → J = 266.67		
	A → K = 120	A → K = 240	250	249
		A → L = 218		
		A → M = 200	200	200
		A → N = 184.615		
		A → O = 171.429		
		A → P = 160	160	160.5
		A → Q = 150		
		A → R = 141.176		
		A → S = 133.33		
		A → T = 126.316		
		A → U = 120.0	120	129

The table also indicates that the drum having a diameter of 8.692 inches cannot be used to produce a scanning density of 480 pels per inch. Therefore, it was also eliminated.

The 4.346-inch-diameter drum provided choices of scan densities as shown in the third column from the left in the table. The values originally suggested by RCA are shown in the next column. The last column shows some arbitrary values generated by stating a desire to have four intermediate scan density samples between resolutions of 200 and 600 pels per inch. This produces a ratio of $\sqrt[5]{3}$ between equal geometrically related steps. By comparing columns 3, 4, and 5 the choices underlined in column 3 appear to be highly satisfactory.

ENCODER BUFFER CIRCUIT

Previous scanning experiments at resolutions of 200 by 200 pels per inch only required a positive-going-edge signal from one of the two quadrature tracks. The present strategy requires the use of both rising and falling edges, both tracks. The technique for accomplishing the combination and pulse generation is shown in figure B11.

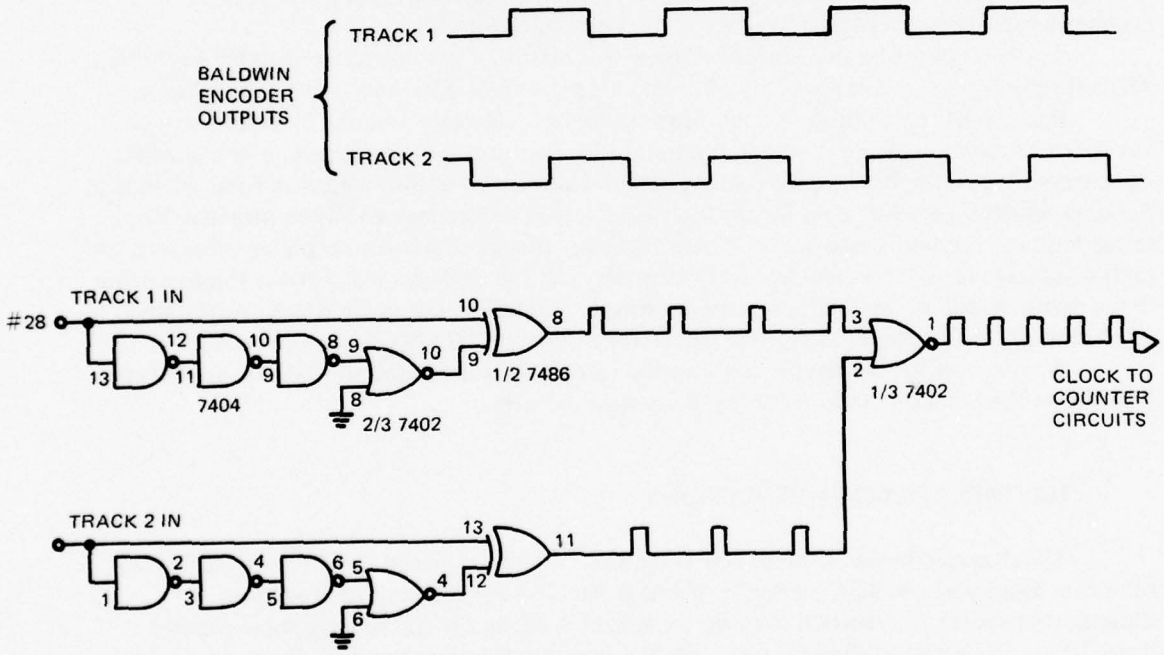


Figure B11. Clock track pulse generator logic diagram.

The resulting set of unmodified pulses is capable of defining a resolution of 2400 pels per inch with the 4.346-inch-diameter drum. With other drum diameters, other resolutions can be obtained with the same pulse stream. In order to reduce the resolution of the acquired image acquisition, it is necessary to count down the pulse stream frequency. Allowing every other pulse to pass (a 2:1 divider), the resolution drops to 1200 pels per inch. Allowing every third pulse to pass (a 3:1 divider) reduces the resolution to 800 pels per inch.

Figure B12 shows a logic diagram and a table of values for a count-down circuit which divides down as far as 20:1, which produces a resolution of 120 pels per inch. Lower resolution requirements present no problem, since the software programs can be used to combine groups of pels in 2-by-2, 3-by-3, or larger groups which can be averaged to represent a single large pel. It should be pointed out that nonuniform resolution images such as 200 by 400 pels per inch can be generated with software programs.

PULLEY COMBINATIONS

Data acquired for full-page images must be stored on magnetic tape, since the single module of semiconductor frame-store memory (FSM) has insufficient capacity for all the data. The acceptance of one scan line by the ICAS is divided into three parts. The first part is the transfer of the 1728 pels from the imager to the FSM. This is done by packing sequences of eight 6-bit pels into 48-bit words in the Memory Control Unit (MCU) and storing the string of words into the FSM until a full scan line is acquired.

The second part of the storage process is the transfer of the composed line of data to the tape unit under the synchronization of the Format Control Unit (FCU). A line number designation is sent as a header for each line transmitted.

The final part of a line storage is the introduction of an interrecord gap between lines. The entire process requires about 50 milliseconds per line of data, regardless of resolution.

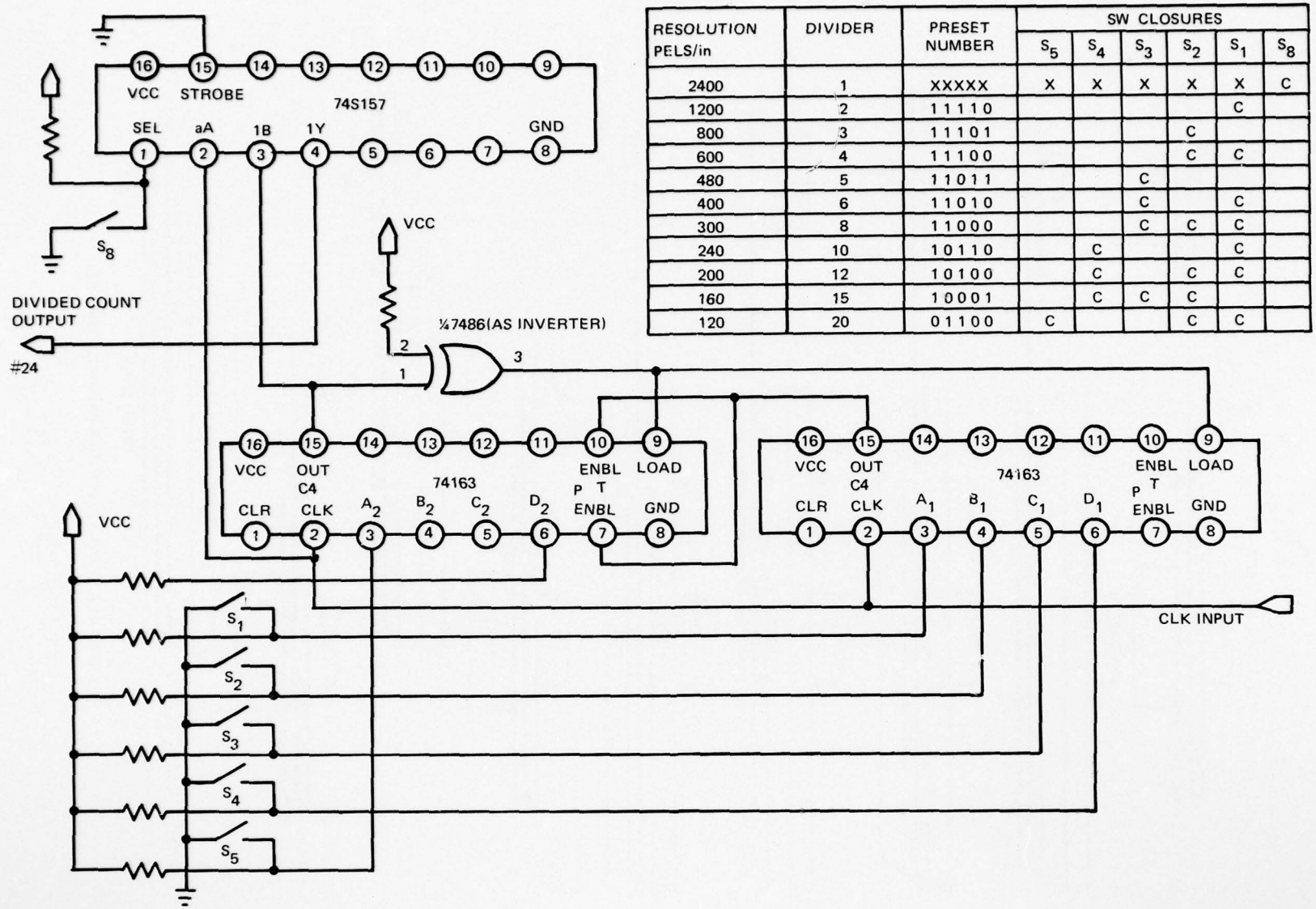
Because of the stiction of some bearings there is a certain amount of irregularity to the speed of rotation at the low speeds required for capture. For this reason a safety factor has been added to the line acquisition rate and a time of 100 milliseconds has been selected as the time allotted per line. This means that any drum rotational speed which provides 10 or fewer lines per second is satisfactory. Selections for the combinations of pulleys required for each resolution have been calculated. Fortunately, all the pulleys made for the large existing drum design could be used with the smaller drum. No pulley was made to accommodate a resolution of 2400 pels per inch since this is not a current USPS/RCA requirement.

Annex A of this appendix contains the calculations for required resolutions. Figure B13 shows the belt connections for the RCA scan densities.

ILLUMINATION MODIFICATIONS

The decrease in the drum diameter caused the image surface to be displaced toward the drum axis by about 4.36 inches. For this reason it was necessary to move the illumination source to maintain the proximity which existed with the large main scanner drum. This was accomplished by removing the high-speed motor temporarily and tapping four mounting holes in edges of the horizontal optical bench slab and simply moving the entire lamphouse down the bench and remounting it.

During the test the acquisitions were made without the cover on the lamphouse. It was felt that there was less modulation of the total brightness at the scan line due to adjacent copy reflection than with the cover on. The Nikon lens used has a very low flare coefficient, so it was concluded that better images can be obtained in this configuration.



RESOLUTION PELS/in	DIVIDER	PRESET NUMBER	SW CLOSURES					
			S_5	S_4	S_3	S_2	S_1	S_8
2400	1	XXXXX	X	X	X	X	X	C
1200	2	11110					C	
800	3	11101				C		
600	4	11100				C	C	
480	5	11011			C			
400	6	11010			C		C	
300	8	11000			C	C	C	
240	10	10110		C			C	
200	12	10100		C		C	C	
160	15	10001		C	C	C		
120	20	01100	C			C	C	

Figure B12. Resolution pulse count divider.

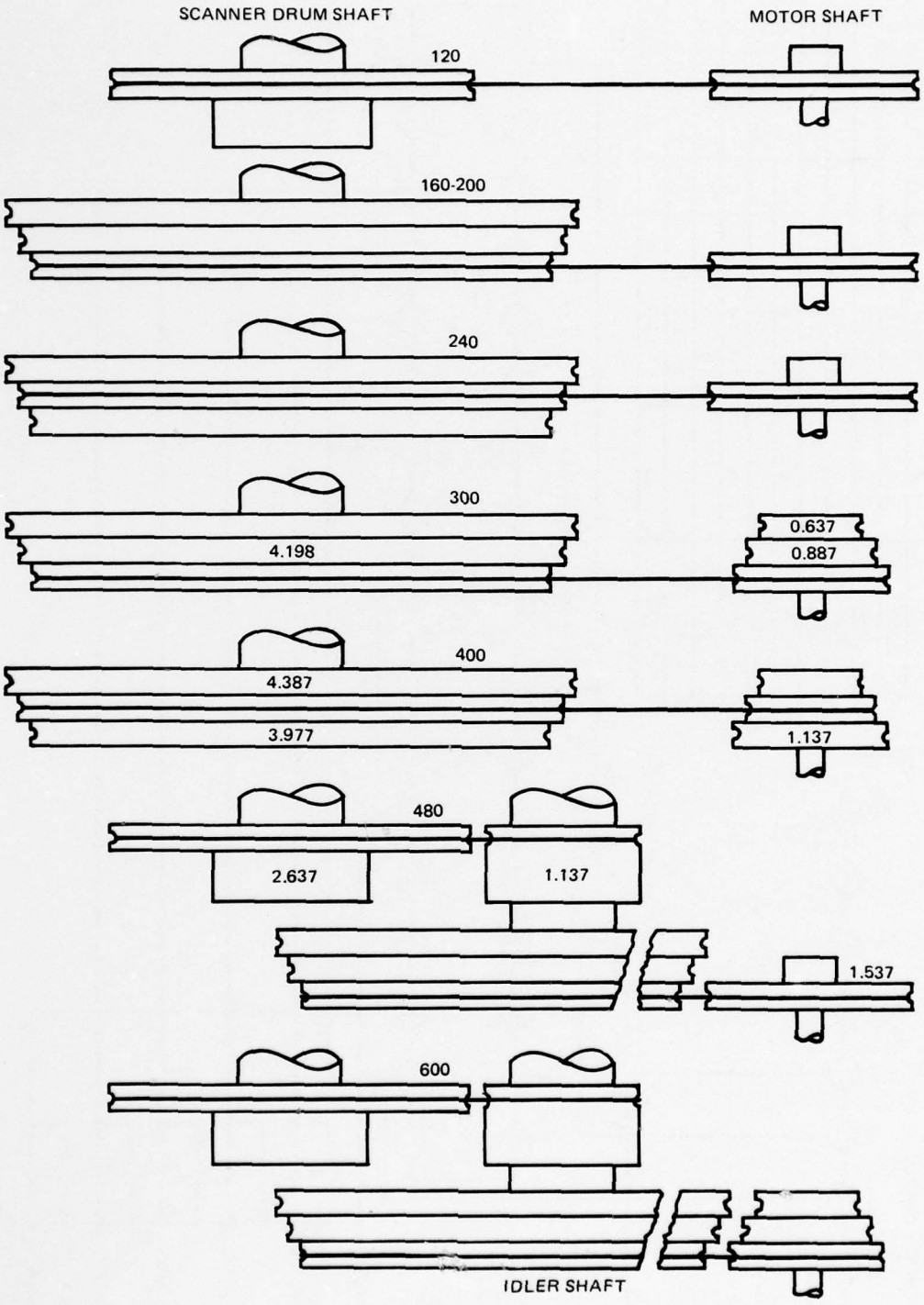


Figure B13. Variable resolution pulley connections.

CALIBRATION PROGRAM GENERATION

For the resolution test, four independently executable software modules are required. These modules are the resolution check routine, white standard acquisition, image acquisition, and correction/analysis.

The resolution check routine is used in conjunction with a special target image and is used during setup for verification of scan density.

The acquisition of the white standard image is simply the capture of 16 lines of data using a plain bar target of a uniformly high-reflectance material. The use of this to compensate for electro-optical anomalies during the acquisition of images has been described in detail in the previous program reports[B1].

The actual acquisition process, once the proper resolution setup has been made, is no different from other routine image acquisitions made in the past. These have also been described in detail in reference B1.

The correction and analysis software for this test was somewhat different from that used in previous procedures. Only a portion of the image may be needed by RCA for the printing. For example, at 120 pels per inch the 8½-inch width can be accommodated by only 1020 pels of scan width. Constants can be entered into the program to select a subset of the captured raw image for illumination correction, analysis, and storage on tape.

The selected portion of the image is compensated for illumination variations and is also analyzed. The Digital Image Analyzer (DIA) is not used for this analysis. Instead, a software program is used to produce the pel brightness statistics (PBS) and first difference statistics (FDS). Only the portion of the image recorded for RCA is included in the analysis.

There is also additional software required at this time to reformat the stored image data into the RCA-readable format; ie, one pel per tape character and one line per tape record. This procedure may also split a corrected image or segment into two equal portions for placement on two separate tapes if the segment is too long for one tape.

[B1] Second Annual Report, Advanced Mail Systems Scanner Technology, NELC TR 2020, October 1976.

SETUP AND CALIBRATION PROCEDURE

RESOLUTION TEST IMAGE

A special resolution target as shown in figure B14 is attached to the drum. This test chart contains black and white bars at a resolution of 10 lines (5 line pairs) per inch. It also contains a resolution wedge having a range of about 40 to 600 lines per inch. The horizontal array of short vertical bars is used to establish the horizontal resolution and focus. The vertical array of short horizontal bars is used to verify vertical resolution.

RESOLUTION ADJUSTMENT

The resolution calibration software is designed to capture an image (onto magnetic tape) which corresponds to an area including 1728 pels in width and 4 inches in height. When the resolution chart is attached to the drum, the vertical portion of the "T" pattern is carefully centered so that the 864th pel in each line falls on the stem.

Once the area image has been stored on tape, the procedure examines one 1728-pel horizontal line approximately 1/8 inch from the top of the test image.

The next step of the routine is to search for the first high threshold which follows the first low threshold beginning approximately 1 inch to the left of the center of the scanned line. Figure B14 indicates the 2-inch segment which is actually used to determine the number of pels acquired in the sample interval. Figure B15 shows how the program begins the search for the first real low-to-high transition then counts the pels received during the next 10 similar transitions. This digital hysteresis loop has been quite successful in avoiding false starts and stops due to test image blemishes, dust, and electrical noise. The resulting count is divided by two to provide the number of pels per inch. This number is stored until the vertical resolution is determined.

A similar process is used to provide a value of resolution in the direction of copy motion. A single pel from each line (pel number 864) is taken from the tape and formatted in an array in the FSM by the Memory Control Unit (MCU). Sufficient samples are taken to provide 10 cycles of the black/white line pairs occurring after the first low-to-high transition of the target column. As before, the pels acquired in the 10-cycle interval are counted and the quantity is divided by two.

At the end of these two routines, the resolution numbers are sent to the front-panel display of the MCU and presented in octal form.

FOCUS ADJUSTMENT

There is some interaction between resolution and focus adjustment. Focus is obtained by stopping the drum motion with a segment of the resolution test wedge in the field of view of the imager. The output of the preamplifier is connected to an oscilloscope and presented on the Y axis with the X axis synchronized to the line rate of the imager. Maximum excursion of the Y amplitude signal is obtained with optimum focus. After focus is obtained,

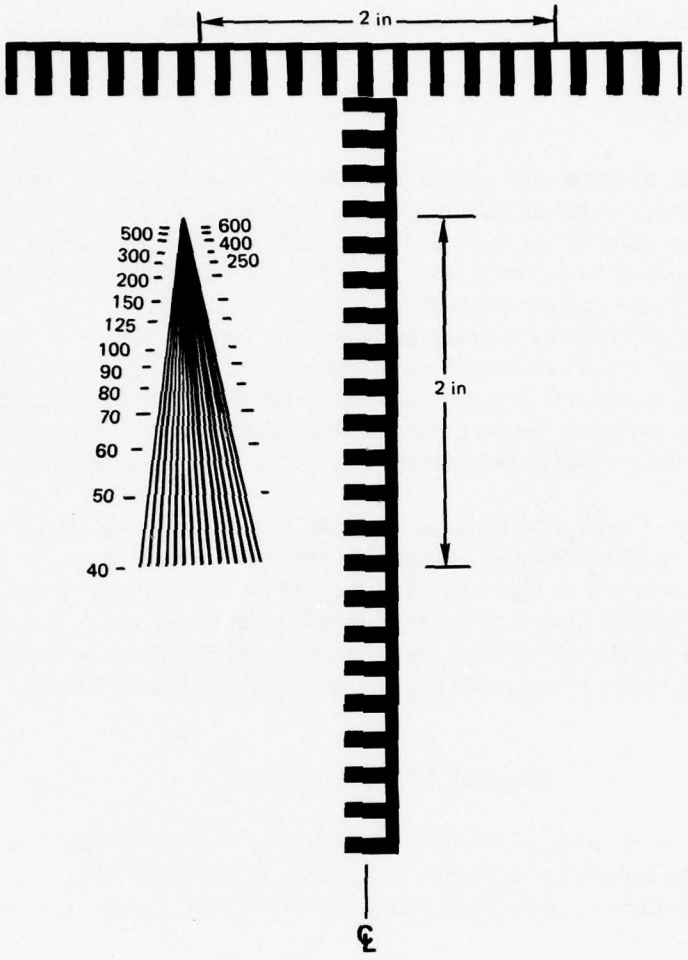


Figure B14. Resolution test target.

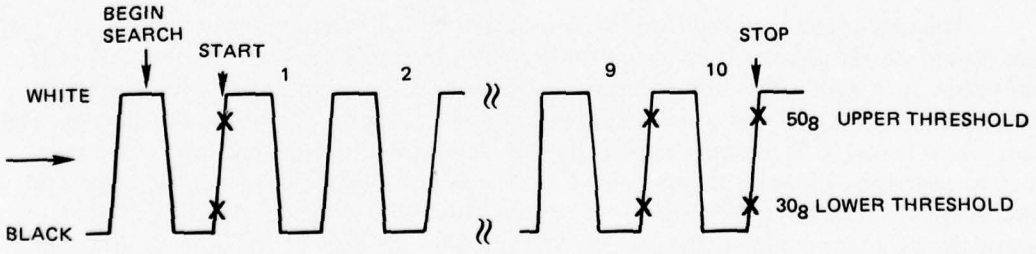


Figure B15. Calibration video thresholds.

the resolution check is rerun and minor adjustments are made in the distance between the imager and the target as required. The process of distance adjustment, focus, and resolution computation is repeated until focus and resolution are both satisfactory.

BRIGHTNESS LEVELS

For usual tests at NOSC, the system is set up in a "prescan" mode. In the prescan mode, the dynamic range of the illumination is set to provide a digital output of all 0's when the scanner is imaging on the black felt "black standard." The analog system gain is set to produce all 1's (level 63 decimal) from the A/D converter when the scanner is imaging on the high-reflectance "white standard."

The above adjustment of brightness levels is made for two reasons. First, the two extremes chosen for the "black standard" and "white standard" ensure that all reflection densities encountered on the test copy samples will be accommodated without exceeding the limits of the A/D converter. Second, the use of a standard setup ensures that the data are based on an absolute reference and that the test can be repeated with almost identical results.

For this series of resolution tests, however, RCA has asked for particular nominal digital values for the recorded levels of background and information. In all samples, the information is dark on a lighter background. The background is reasonably uniform for all samples. However, the reflection density of the information has considerable variation. For these tests, RCA has asked that the nominal background brightness be recorded at level 52 or greater. The nominal brightness level of the information (inks) averaged above level 9.

ACQUISITION OF IMAGES

Once the spatial frequency and focus of the test bed have been established, all the test documents can be captured at a specific resolution. Because of the large volume of data involved in the acquisition, a carefully sequenced and documented procedure was generated and followed.

RAW IMAGE CAPTURE

The test images received from RCA were all one-of-a-kind original documents on plain bond paper. Consequently, they were handled very carefully since they were used at least nine times, once with each resolution setup. The test drum was wrapped with plain bond paper extending both sideways and lengthwise beyond the perimeter of the documents. The copies were mounted as squarely as possible with single-sided transparent tape. Care was taken to overlap the tape on the document as little as possible and to prevent smudges and other cosmetic defects on the masters. Care was also taken to ensure the positional accuracy of the documents so that the pels per line and lines per page provided to RCA would contain only data from the copies insofar as possible.

Gain and level of the preamplifiers were set for each document so that the nominal brightness levels of the background and information were 52 and 12, respectively.

Each document was acquired in raw form in the normal tape format used at NOSC for tape storage. This provides somewhat higher-density packing than the one-character (pel)-per-byte RCA-compatible format. The increase in packing density improves the possible tape acquisition rate. The entire 1728-pel-per-line output of the imager was stored on the tape during the capture. Nonrelevant pel data were stripped from the data during subsequent processing.

SEQUENCE OF ACQUIRED RESOLUTIONS

Since the test bed was already set up for acquisition at a resolution of 200 by 200 pels per inch, the documents were initially scanned at this resolution. A total of 2200 lines was acquired which encompassed the entire 11-inch length of the document. Segments from each image were displayed on the Conrac monitor to verify that the data were acquired properly.

The next series of acquisitions was made at a scan density of 160 by 160 pels per inch. Only 1760 lines of data are required per 11-inch page. As before, 1728 pels were captured even though only 1360 pels contain data pertinent to the test samples. Table B2 defines the image segment dimensions for all the images acquired.

A series of acquisitions was made at 120 by 120 pels per inch. Only 1320 lines were needed and the actual copy only required 1024 pels per line to cover the document width, although the entire 1728 pels per line were again stored on tape in the NOSC format. This low resolution was just barely accommodated by the large drum test bed (LDTB) because of the relatively long distance from lens to object when imaging with the 55-mm lens. Lower-resolution or longer-focal-length lenses might require an extension track and jumper cables to increase the lens to object distance.

The next in the sequence of resolutions to be captured was 240 by 240 pels per inch. At this resolution it is not possible to scan the entire 8½-inch page width with a 1728-pel imager. Therefore, the images were bisected at predetermined cut points. The halves of each image were then affixed to the drum and scanned sequentially. The images were rotated 90 degrees so that the 5½-inch width of the image could be accommodated by the 1728-pel imager. The 8½-inch length will be available on record by scanning 2040 lines each containing 1728 pels (1320 pels required).

The same bisected images were sequentially remounted and scanned after the setup for 300-by-300-pel-per-inch acquisition was verified. At this scanning density, 2550 lines at 1728 pels per line were recorded (1650 pels were required).

At the next desired spatial scanning frequency, 400 by 400 pels per inch, the 1728-pel imager cannot accommodate the 5½-inch width of the bisected page. It is therefore necessary to redivide the bisected image segments into halves. The resulting 2¾- by 8½-inch strips were then scanned across the narrow dimension. A total of 3400 lines of 1100 pels each was acquired to assure that the necessary 1100 pels would be available for transfer to the RCA formatted tapes.

The ¼-page segments are sufficiently narrow to allow acquisition with the 1728-pel imager at the two remaining resolutions, 480 by 480 and 600 by 600 pels per inch. Although the full 1728-pel width was recorded, the ¼-page segments required 4080 lines at 1320 pels for the 400 resolution and 5100 lines at 1650 pels for the 600 resolution. RCA requested

TABLE 2. IMAGE SEGMENT DIMENSIONS.

Resolution, Pels per Inch	Scanned Segments Per Document	Relevant Pels Per Line	Acquired Pels Per Line	Files Per Segment	Lines Per Segment	Relevant Pels Per Segment	Acquired Pels Per Segment	Relevant Pels Per Document
120	1	1020	1024	1	1320	1346400	1351680	1346400
160	1	1360	1360	1	1760	2393600	2393600	2393600
200	1	1700	1704	1	2200	3740000	3748800	3740000
240	2	1320	1320	1	2040	2692800	2692800	5385600
300	2	1650	1656	1	2550	4207500	4222800	8415000
400	4	1100	1104	1	3400	3740000	3753600	14960000
480	4	1320	1320	2	4080	5385600	5385600	21542400
600	4	1650	1656	2	5100	8415000	8445600	33660000*

*At 6 bits per pel = 201 960 000 bits per image

that these records at the 480 and 600 resolutions be further subdivided when recorded in the RCA format so that the limits of the printer capacity would not be exceeded. For this reason file marks were inserted after 2040 and 2550 lines of record for the tapes at 480 and 600 pels per inch, respectively.

IMAGE CORRECTION, ANALYSIS, AND TAPE REFORMATTING

Image correction is accomplished by utilizing the results of scanning the "white standard" which were obtained at the beginning of each setup. These responses prestored on a pel-by-pel basis across the 1728-pel imager provide a series of responses which can be used to provide at least a first-order correction factor for each elemental response of the imager to a uniform bright target under the conditions of illumination which were used in acquiring the test images. This process has been described in detail in reference B1. For these acquisitions, a set of 16 lines was acquired across the white standard target to produce 10-bit values for each of the 1728 pel positions. The 10-bit correction table was used on all images.

The image analysis consisted of acquiring the pel brightness statistics (PBS) and first difference statistics (FDS) of only the areas which were to be transferred to the RCA formatted tapes. The restriction to the areas of record conserved processing time and allowed the analysis data to be fully relevant to the image data submitted to RCA for printing.

The PBS are obtained by counting the number of occurrences of each of the possible 64 values of brightness obtained in an image or image segment. The number of pels which will be obtained in each image is shown in table B2. It should be noted here that the exact number of pels per line which were analyzed and reformatted may be in excess by four pels (as in the case of resolutions of 120, 200, and 400) or six pels (as in the case of resolutions of 300 and 600). This acceptance of a few extra pels per line greatly simplified the correction, analysis, and reformatting algorithms since it operated on all eight pels in each 48-bit memory word, including those on the borders of the useful areas. The excesses do not appreciably alter the statistics and allow a few pels of overlap which may be useful in reassembling the segments. As an example, 3 748 800 pels were used at 200 by 200 pels per inch rather than 3 740 000, an excess of 0.235%. In almost all cases the brightness values of these excesses are those of corrected background reflectance.

The FDS statistics include the same areas defined above. First differences are obtained by calculating the absolute value of the difference in brightness between an acquired pel and its predecessor pel in the scanned line. The number of times each difference value is obtained is recorded for each image or image segment. These data can provide histograms on the effects of scanning density on pel-to-pel brightness differences.

The NOSC preferred tape format for the storage of image data provides a high packing density of pel data. The memory words of 48 bits normally contain eight 6-bit pels. The Kennedy tapes utilize 8 bits per character. The high packing density is achieved by storing data on all eight tracks of the tape. Since the MCU handles the packing and unpacking process with very little processing time, and the tape mechanical motion requires a significant amount, the high density yields faster operation and more data capacity per tape.

The format established by RCA for use with the printer is very simple. One pel is stored on each tape character (byte). The least-significant bit of data is stored on track 0 and the most-significant bit (of 6-bit amplitude quantization) is stored on track 5. Tracks 6 and 7 are not used.

A routine was written at NOSC to read data, line by line, from the NOSC standard format, perform the correction, accumulate the analysis data, reformat the corrected data, and write the pertinent results on the deliverable tape. The process required about 40 minutes per segment.

RESULTS

IMAGES

At the time this report was generated, RCA had not completed the printing of the image data submitted by NOSC. When all segments have been printed in bilevel form, RCA plans to send the masters to a reliable source for composition of original-scale masters of each of the nine documents. High-resolution lithograph plates will be made from these, and a number of samples will be printed on quality bond paper. Most of these will be submitted as sets for acceptable cosmetic evaluation. A few will be used by RCA for an internal assessment.

At considerable special effort, RCA accommodated a NOSC request for some early samples which could be included in this report. These are prints of the sample designated as Image-S. This sample contains a most diversified array of copy, such as logos, fine type, handwriting, and graphics.

The process of producing the enclosed figures consisted of numerous steps which would not be used in the normal image printing technique for USPS mail images. The data were acquired on an Optimation drum printer. This printer has provisions for writing at 254 pels per inch (10 pels per millimetre) or 508 pels per inch (20 pels per millimetre). Spot sizes for the two values are 3.937 mils (100 micrometres) or 1.968 mils (50 micrometres). Grey scale negatives were made by allowing the intensity of illumination of the writing spot to vary proportionally to the 6-bit pel values recorded on the NOSC tapes. Thresholded values were obtained by producing saturation and extinction values of the illumination as a function of the most-significant bit (MSB) of the NOSC tapes.

NOSC was then given duplicate black and white negatives and copies of contact prints of the masters. The contact prints were captioned and mounted on heavy cardboard at NOSC and given to the photo lab for copy at a dilated or reduced scale to cause the report negatives to have a 1:1 dimensional relationship with the original. Master plates were then made for the production of pages in this report. The 200-by-200-, 240-by-240-, and 600-by-600-pel-per-inch magnification ratios were 1.27:1, 1.058:1, and 0.846:1, respectively. It is obvious that much of the resolution gained by the higher spatial frequency scanning has been lost in preparing these samples. Nonetheless they are presented as examples of the test.

Figure B16 is the result of printing the illumination-corrected image in grey-scale form using the digitized brightness levels. The image was acquired at 200 by 200 pels per inch and appears to be a faithful reproduction of the reflection density of the master image

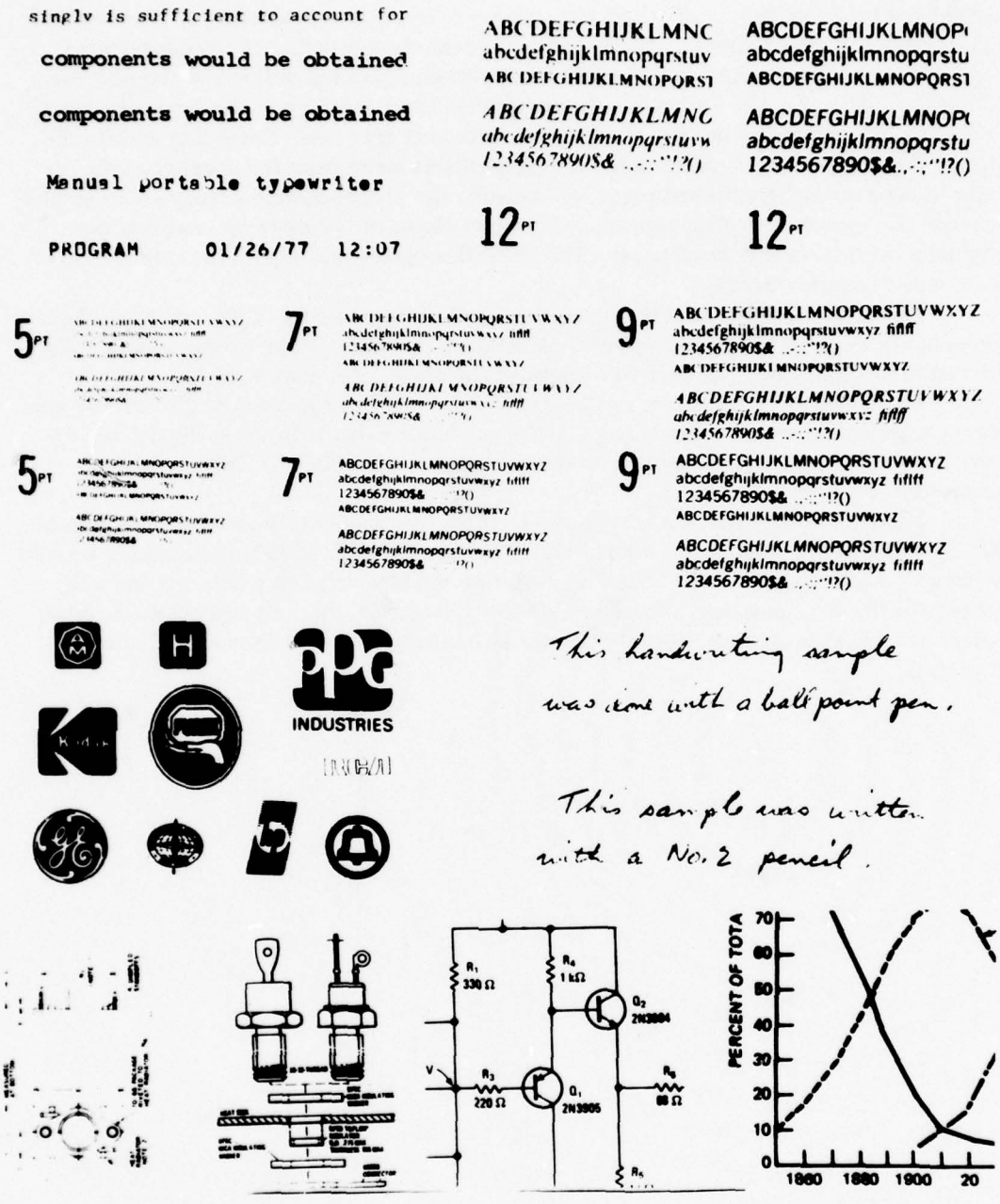


Figure B16. Test image designated S, 200 by 200 pels per inch, grey scaled.

illuminated for broadband visible spectral response. The master is actually a "paste-up" of a number of sample specimens. Variations in the reflection densities of the background papers of the various specimens are easily recognizable, as are the outlines of the paste-up perimeters. Although the nominal background reflectance level lies in the range of level 52 to 63, the background of the reproduction has a distinct grey cast. Recording with background levels closer to 63, printing the sample positives made from the negatives with less exposure and on higher-contrast paper, or adjusting the printer dynamic range could greatly improve the appearance of the reproduced sample. Some of the paste-up swatches were originally printed on thin bond paper. The bleed-through of printing on the reverse side of the samples is quite obvious.

Figure B17 is a reproduction from the thresholded negative. There are some slight traces of the edges of the paste-up, but the image is a reasonable copy of the original. More discussion of figures B16 and B17 will follow in the section on image analysis.

Figures B18 and B19 are included to show the results of imaging at 240 by 240 pels per inch, grey scale and thresholded, respectively. Because of the losses in the document preparation of this report, no significant differences from the 200-by-200-pel-per-inch acquisitions are apparent.

Figures B20 and B21 are composites of the image segments made at a resolution of 600 by 600 pels per inch. Some unevenness in the backgrounds of the segments can be seen in the grey-scale version. The increase in resolution is not significantly better than in the versions of the same document imaged at 200 by 200 and 240 by 240 pels per inch. Some differences can be seen in the copy negatives, particularly around the small typeset alphanumerics.

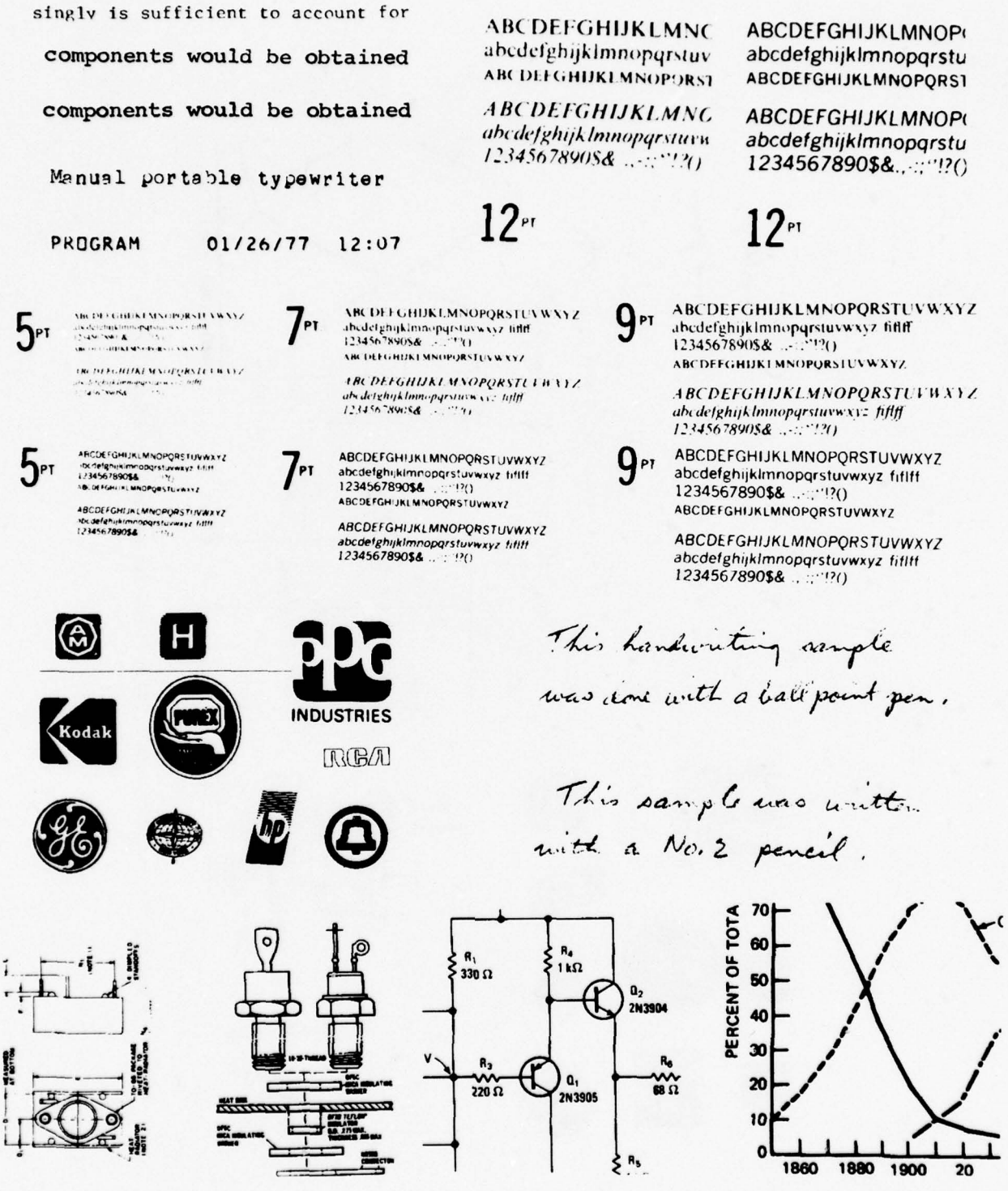


Figure B17. Test image designated S, 200 by 200 pels per inch, thresholded.

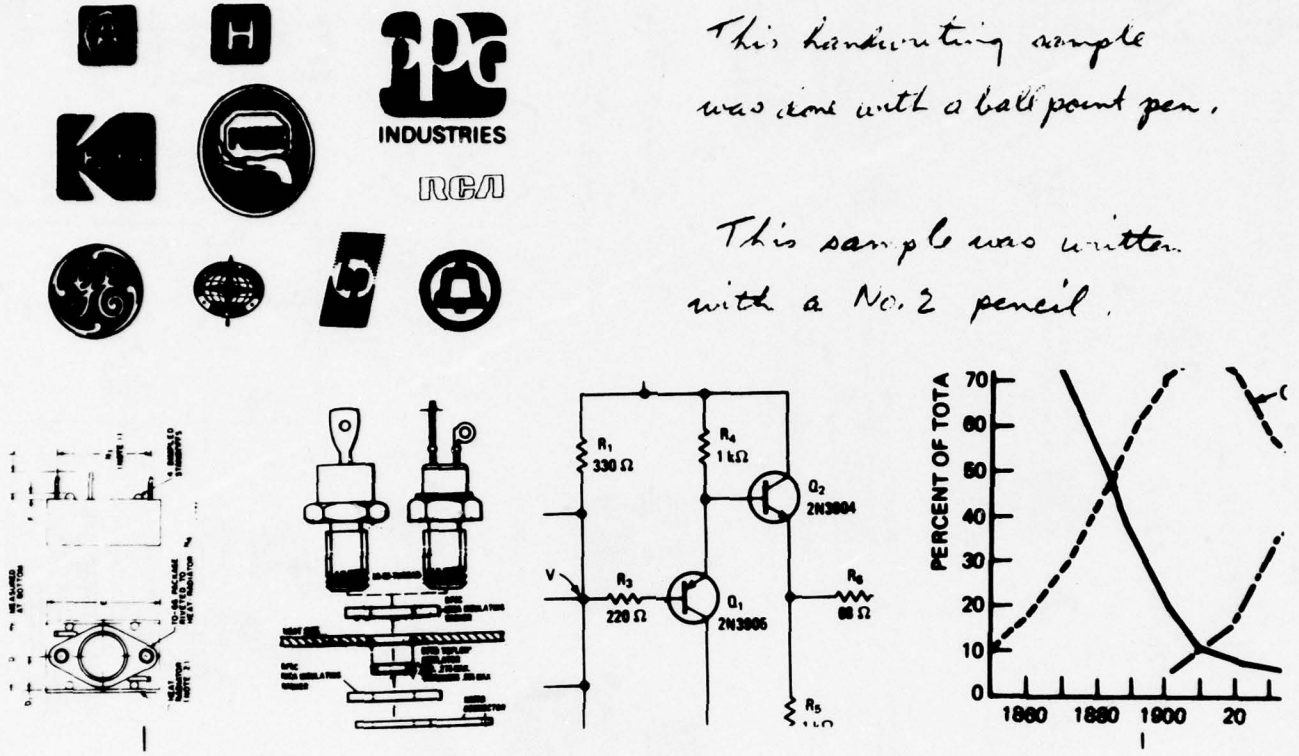


Figure B18. Test image designated S, 240 by 240 pels per inch, grey scaled (lower half).

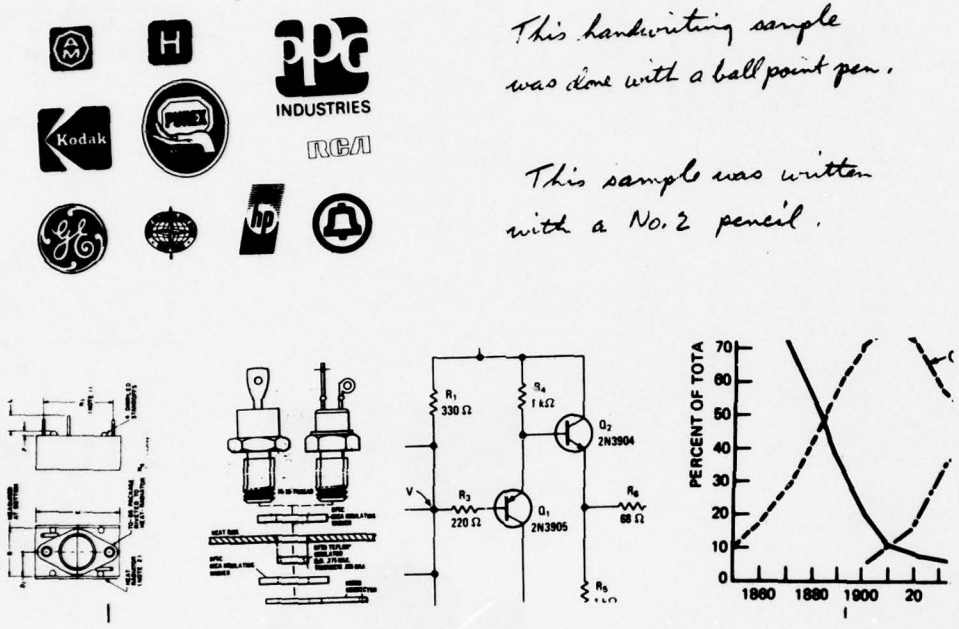


Figure B19. Test image designated S, 240 by 240 pels per inch, thresholded (lower half).

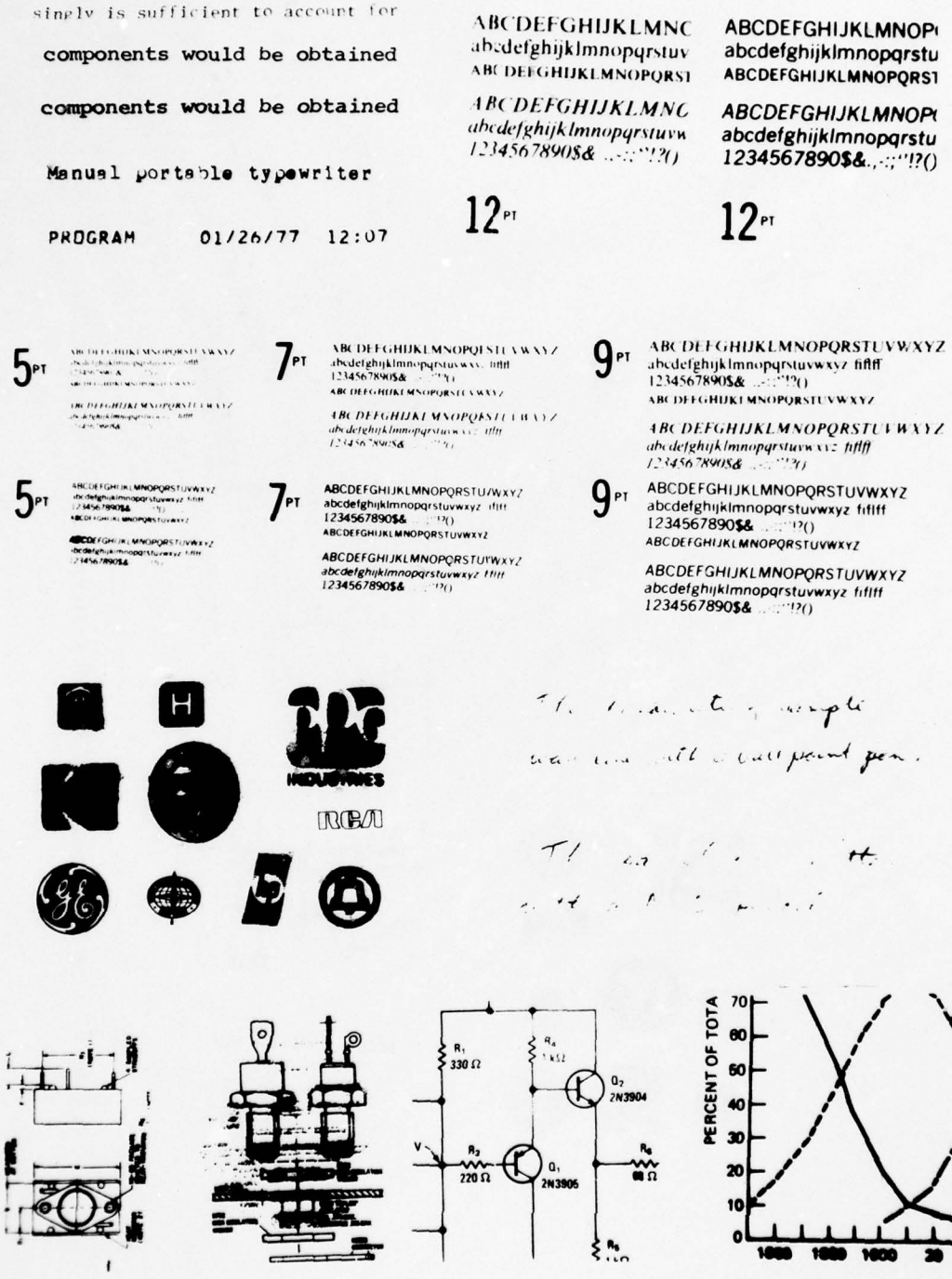


Figure B20. Test image designated S, 600 by 600 pels per inch, grey scaled.

singly is sufficient to account for

components would be obtained

components would be obtained

Manual portable typewriter

PROGRAM 01/26/77 12:07

ABCDEFGHIJKLMNC
abcdefghijklmnopqrstuv
ABCDEFGHIJKLMNOPQRST

ABCDEFGHIJKLMNC
abcdefghijklmnopqrstuvw
1234567890$& .,-:;"'!?()

12PT

ABCDEFGHIJKLMNOP
abcdefghijklmnopqrstu
ABCDEFGHIJKLMNOPQRST

ABCDEFGHIJKLMNOP
abcdefghijklmnopqrstu
1234567890$&.,-:;"'!?()

12PT

5PT ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz fifffl
1234567890 &
ABCDEFGHIJKLMNOPQRSTUVWXYZ

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz fifffl
1234567890$&

7PT ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz fifffl
1234567890$& .,-:;"'!?()
ABCDEFGHIJKLMNOPQRSTUVWXYZ

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz fifffl
1234567890$& .,-:;"'!?()

9PT ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz fifffl
1234567890$& .,-:;"'!?()
ABCDEFGHIJKLMNOPQRSTUVWXYZ

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz fifffl
1234567890$& .,-:;"'!?()

5PT ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz fifffl
1234567890$&
ABCDEFGHIJKLMNOPQRSTUVWXYZ

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz fifffl
1234567890$&

7PT ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz fifffl
1234567890$& .,-:;"'!?()
ABCDEFGHIJKLMNOPQRSTUVWXYZ

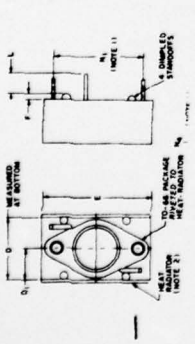
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz fifffl
1234567890$& .,-:;"'!?()

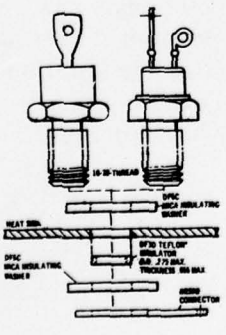
9PT ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz fifffl
1234567890$& .,-:;"'!?()
ABCDEFGHIJKLMNOPQRSTUVWXYZ

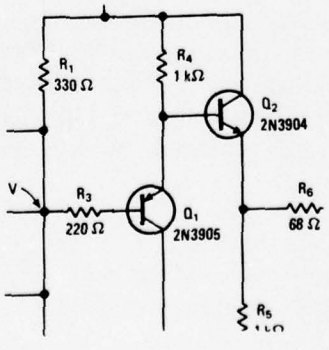
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz fifffl
1234567890$& .,-:;"'!?()

This handwriting sample was done with a ball point pen.

This sample was written with a No. 2 pencil.







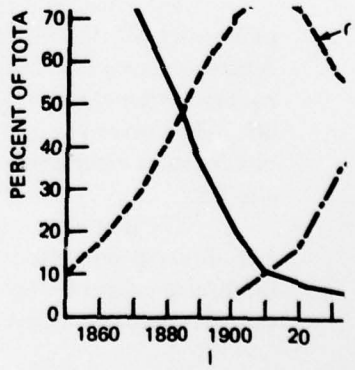


Figure B21. Test image designated S, 600 by 600 pels per inch, thresholded.

ANALYSIS

Two types of analyses were run on each image at each resolution setting. Where the images were obtained in segments, the sums of the pair or four quarters were accumulated to develop the final tallies and histograms which follow.

Figures B22 through B29 are a series of pel brightness statistics (PBS) for Image S resulting from an analysis of acquisitions made at all the requested spatial frequencies. Figure B22 shows the distribution of brightness levels for the image acquired at the lowest spatial frequency of the series, 120 by 120 pels per inch. The brightness level which occurs most frequently is level 55. From associated tabular data (not published, but available), there are 116 004 pels of this brightness level. The total number of pels in the image as listed in table B2 is 1 351 680.

At the right side of the histogram a peak exists at brightness level 14. There are 7587 pels having this brightness. A second peak exists at level 9, this one having a total of 6265 pels. There are six saddle points in the histogram. One of these is at level 11. The other five are at levels 16, 20, 24, 28, and 32. These latter values have the appearance of being caused by nonuniform response of the A/D converter. A subsequent review of other histograms tends to refute this as a cause. The other possible reason for the saddle points may be reflectance sources of different values such as ball point pen, pencil, and bleed-through levels as well as the inks used in the printing process. The two major peaks on the dark (low) end of the histogram are probably two different types of inks.

Figure B23 is an analysis of the same image scanned at 160 by 160 pels per inch and contains many of the features found in figure B22. The six saddle points still exist. This location has shifted, which somewhat confirms the opinion that they are data dependent and not an anomaly of the A/D converter. The nominal background brightness has been maintained above the value 52. The darkest few pels are still at level 5.

Figure B24, which is an analysis made from imaging at 200 by 200 pels per inch, contains the two major responses of ink levels at levels 9 and 13. The data also show two distinct additional peaks at levels 21 and 31. No explanation has been found for the occurrence of these at this scanning density at the exclusion of all others. The stem on a standard typed character is approximately 2.2 pels (0.011 inch). Perhaps the line width on some of the fine printed matter is such that the minimum response from a character stroke of a printed level falls at either level 21 or 31 for different sizes of type. In other words, these should be the lower excursions of the modulation transfer function (MTF) cycles at these spatial line widths.

The remaining analyses shown in figures B25-B29 follow a more traditional and familiar form of the histogram which results from scanning bilevel (black and white) images. A strong response is indicated in the vicinity of level 52 representing the reflectance of the background and a second peak around level 8 or 9 resulting from the contribution of the ink. The curves generally are displaced upward with increasing scanning density due to the rapidly increasing number of pels per image. A scale change has been made on figures B28 and B29.

The next series of figures, B30–B37, resulted from analyzing the data to obtain first difference statistics (FDS). First difference statistics are generated by comparing the brightness value of a pel with the value of the pel immediately following. For example, if the 301st pel in a scan line had a brightness value of 27 and the 302nd pel brightness was

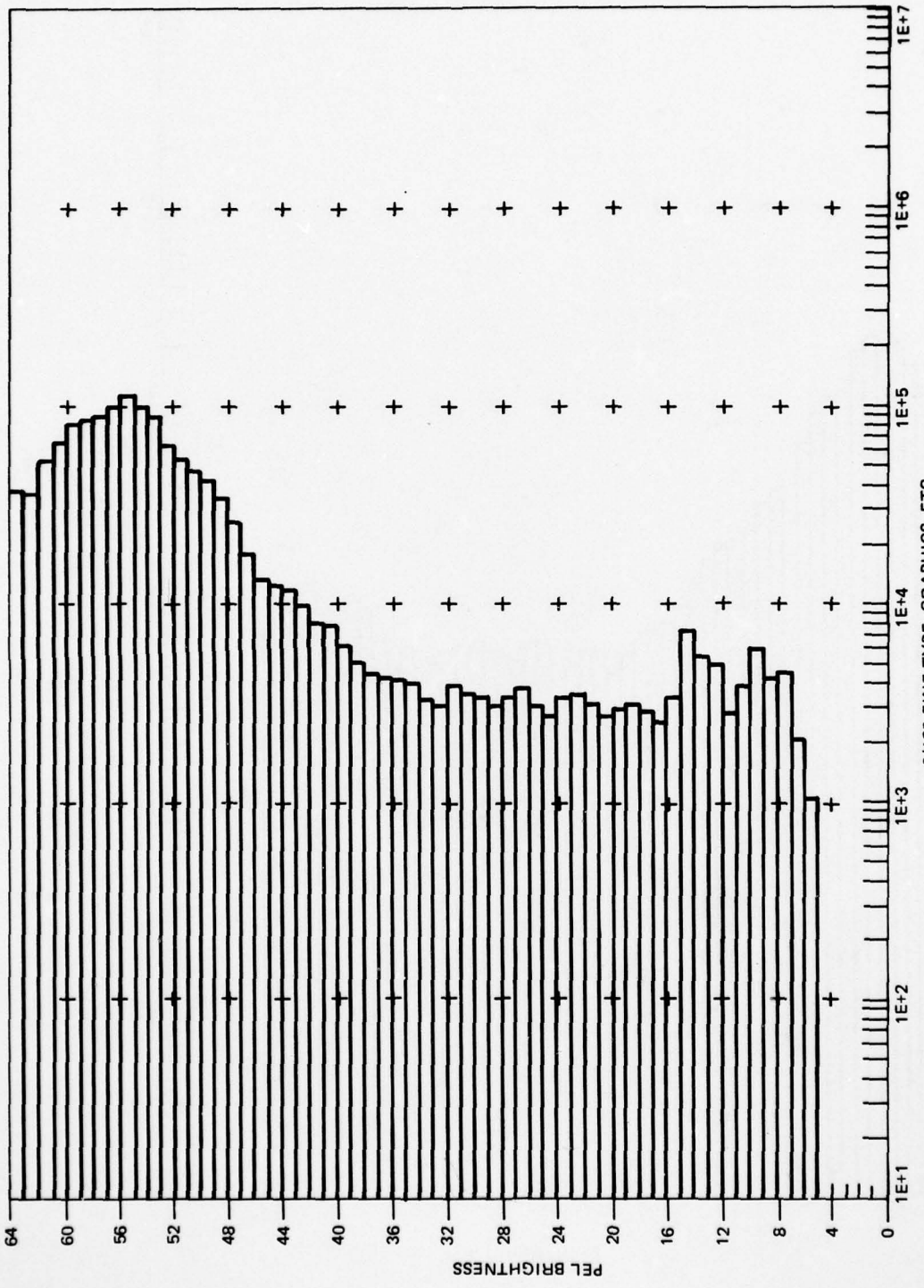


Figure B22. Pel brightness statistics, 120 by 120.

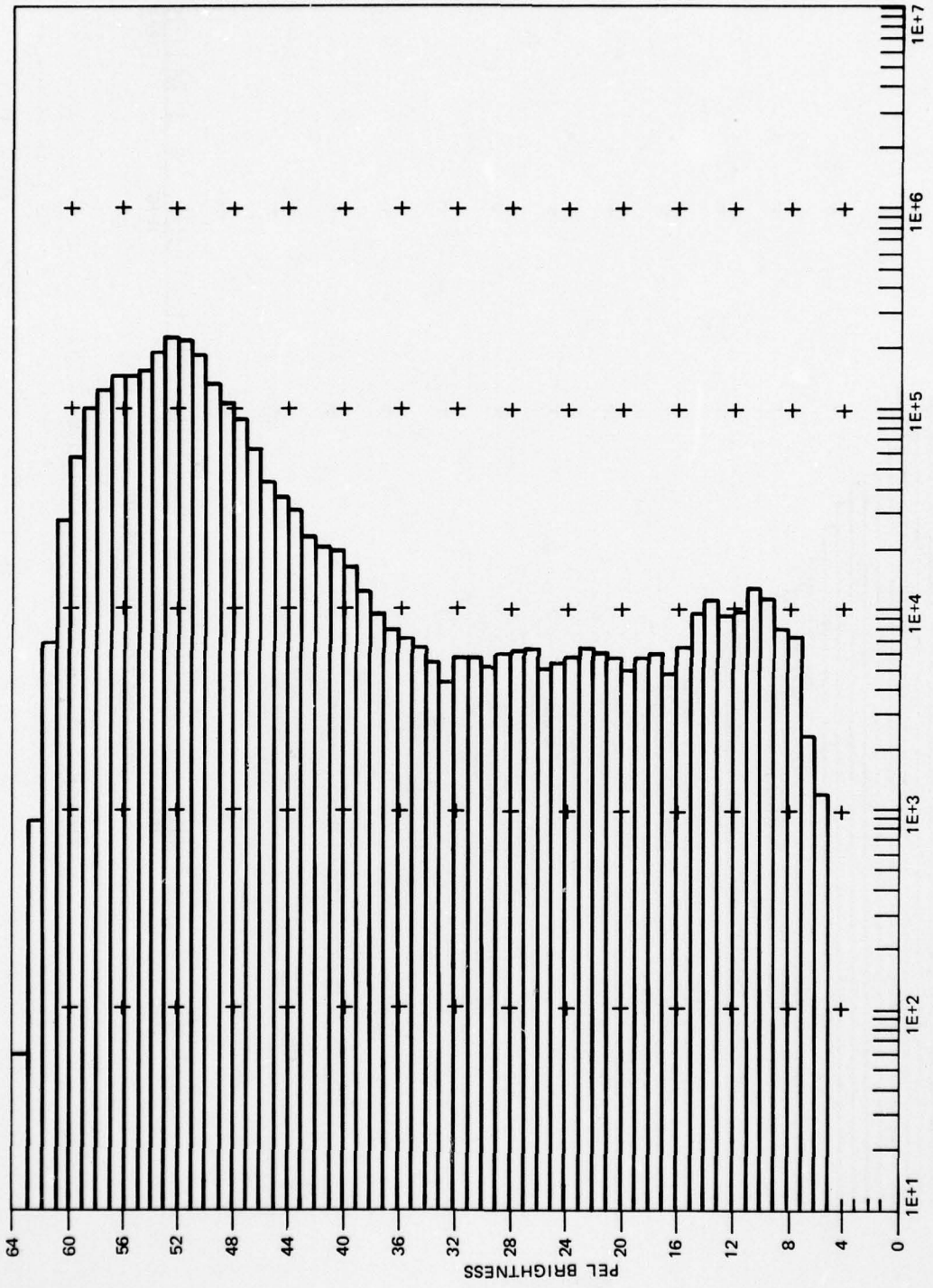


Figure B23. Pel brightness statistics, 160 by 160.

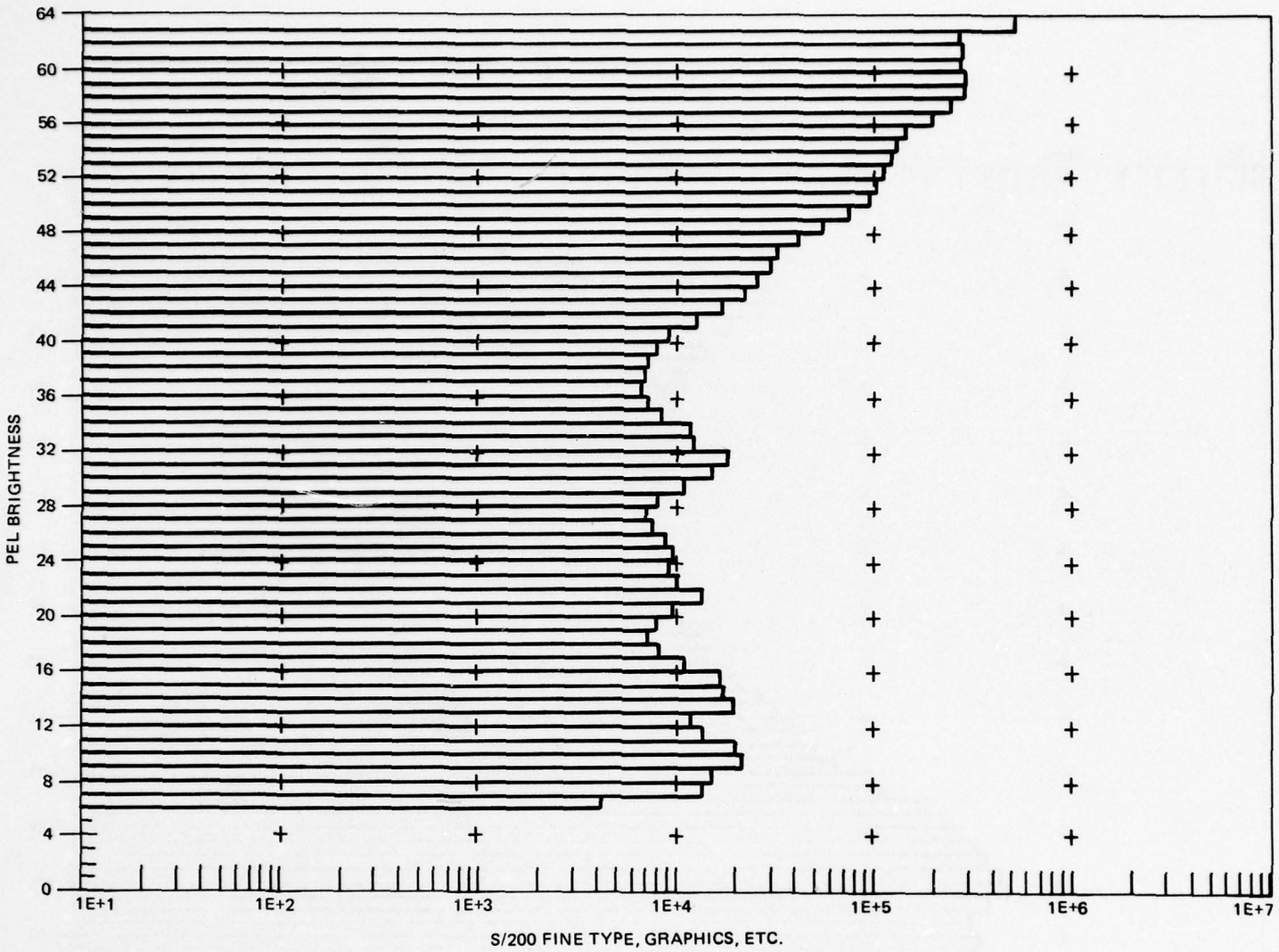


Figure B24. Pel brightness statistics, 200 by 200.

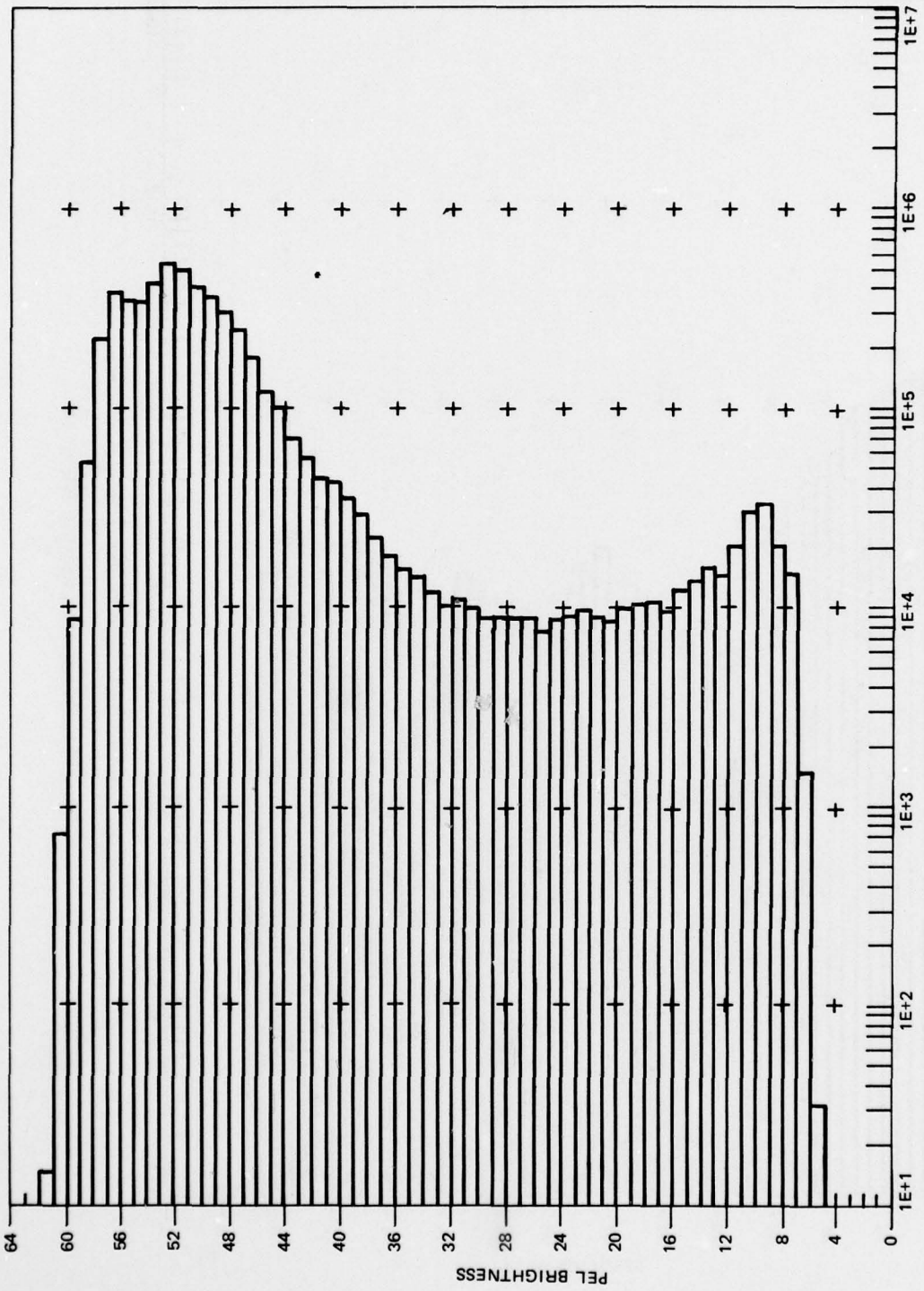


Figure B25. Pel brightness statistics, 240 by 240.

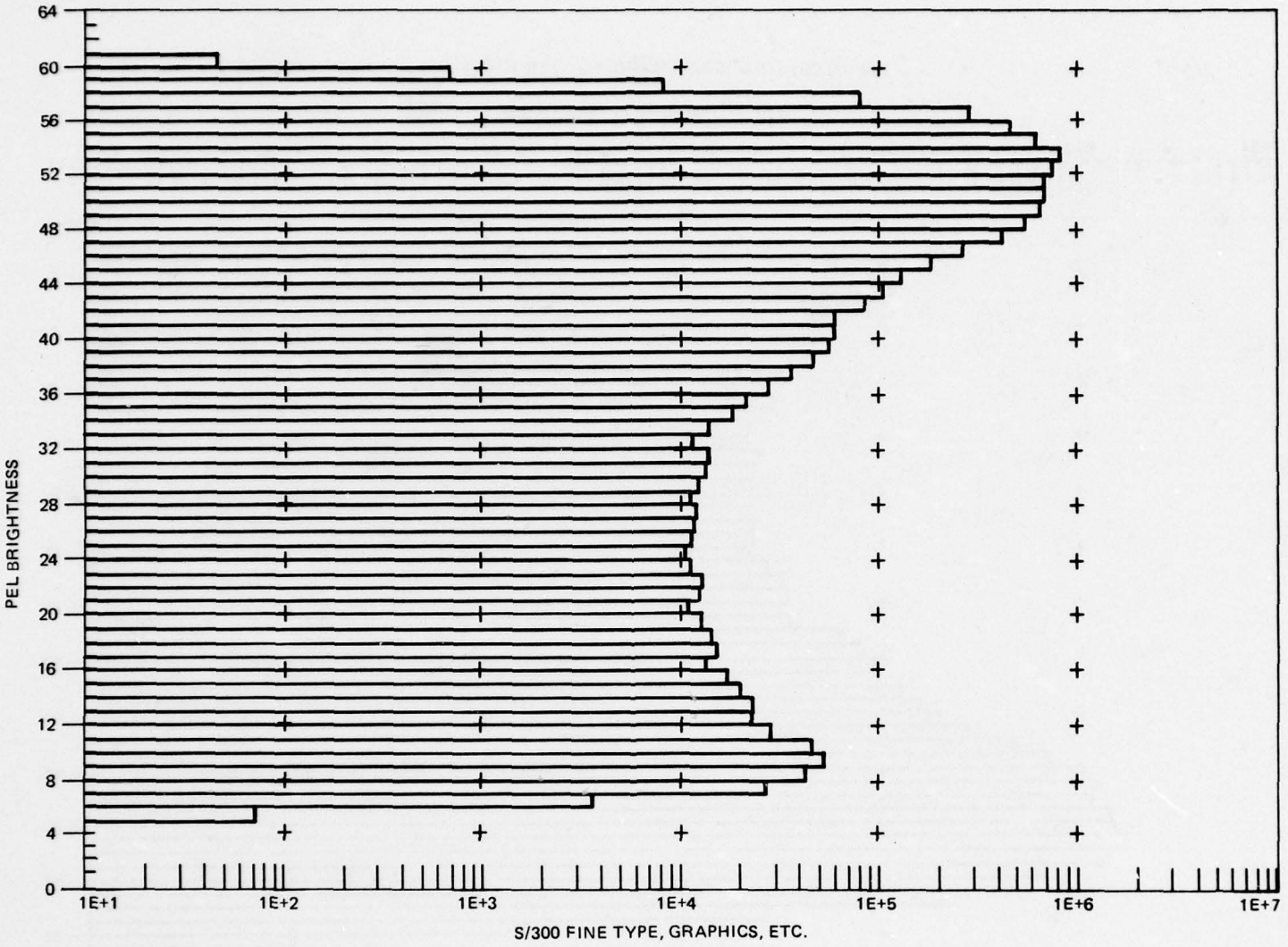


Figure B26. Pel brightness statistics, 300 by 300.

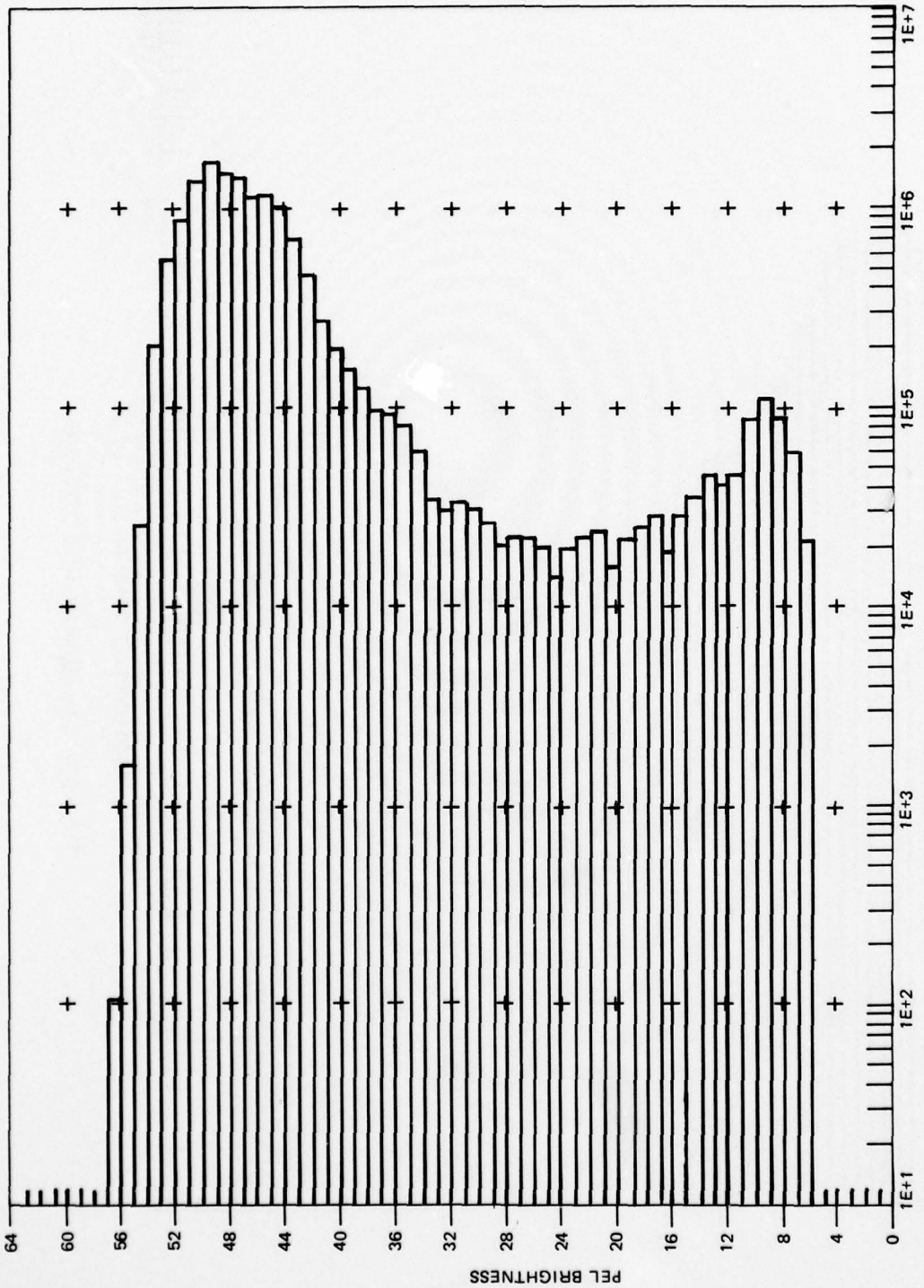


Figure B27. Pel brightness statistics, 400 by 400.

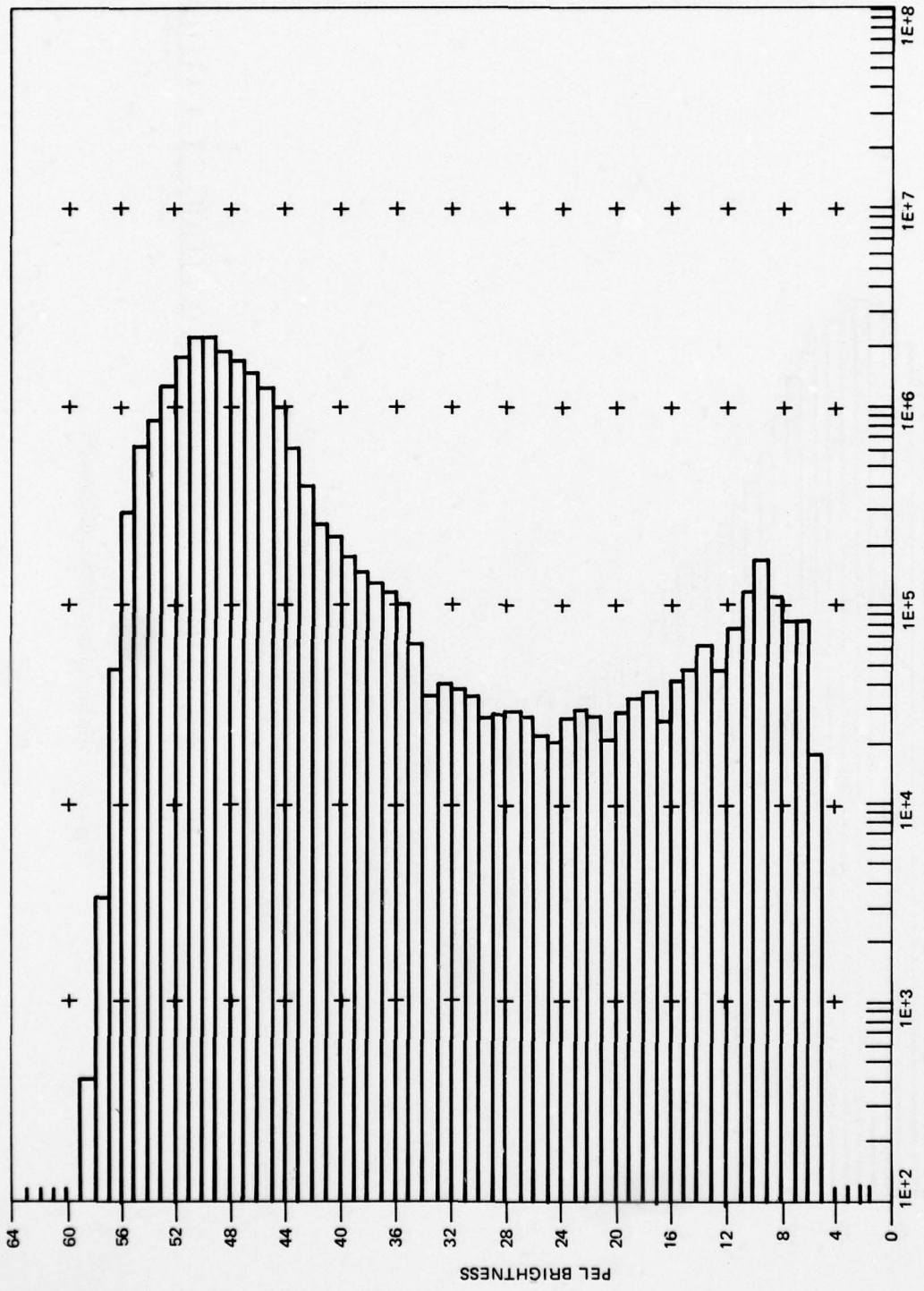


Figure B28. Pel brightness statistics, 480 by 480.

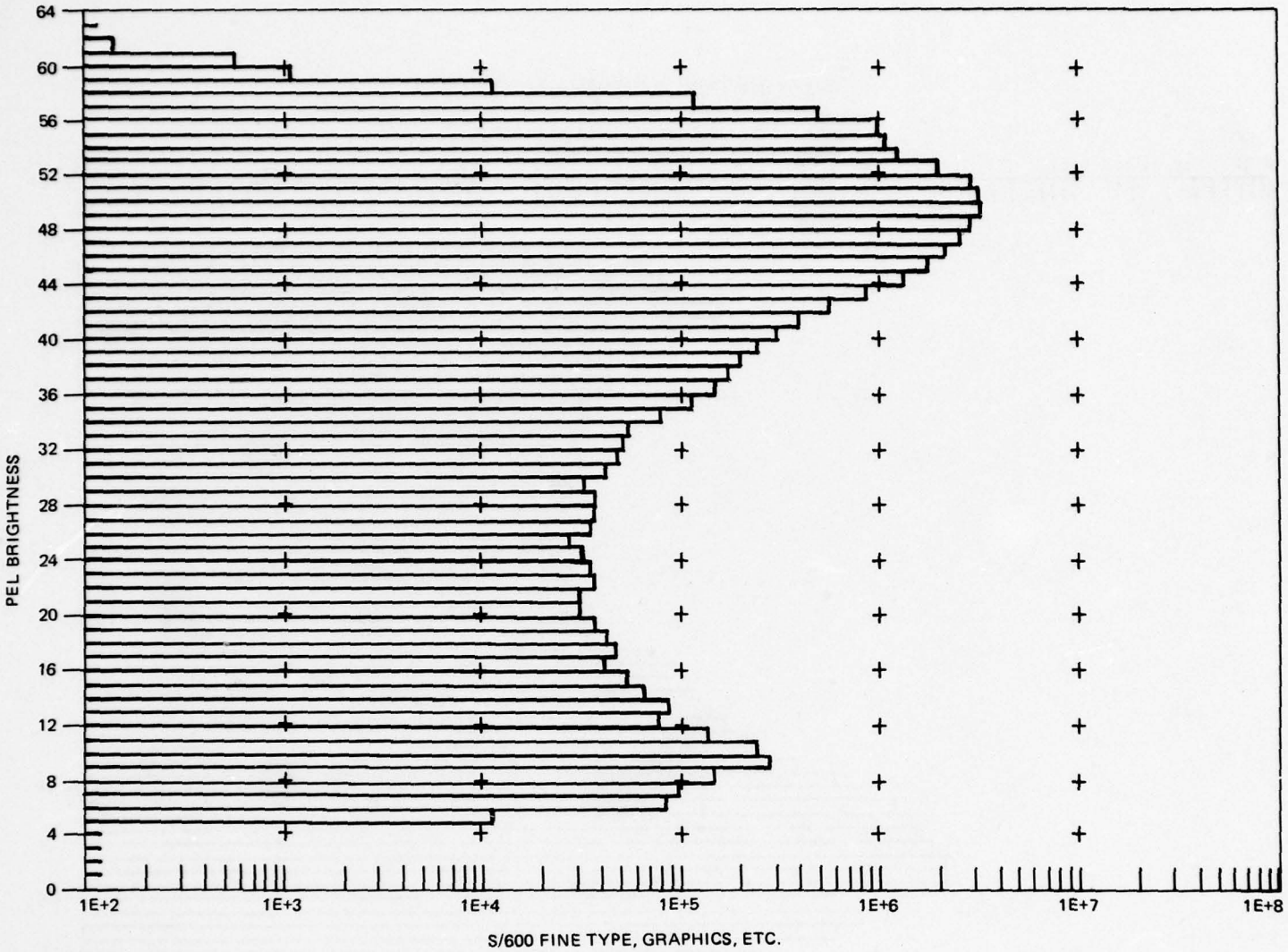


Figure B29. Pel brightness statistics, 600 by 600.

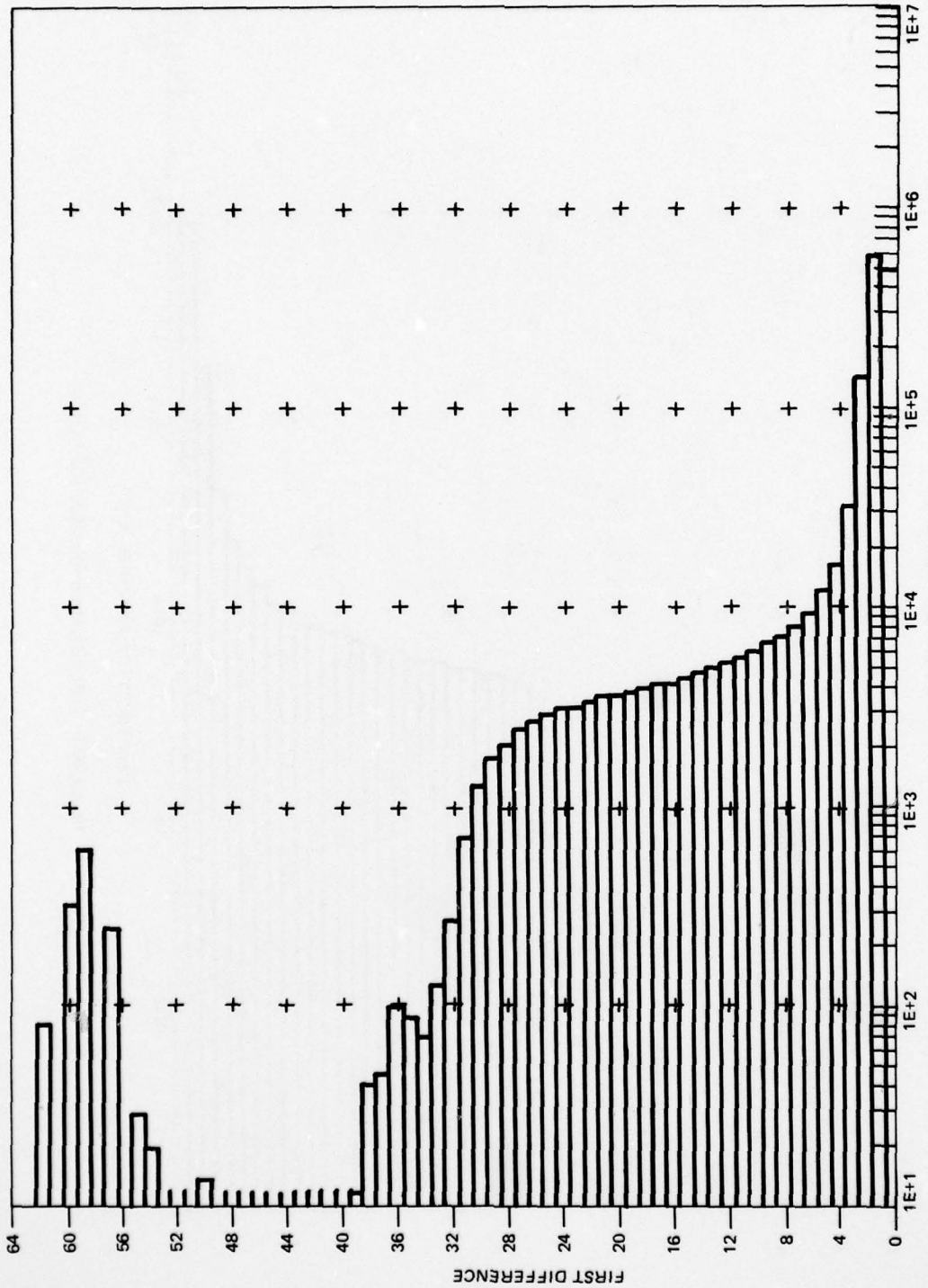


Figure B30. First difference statistics, 120 by 120.

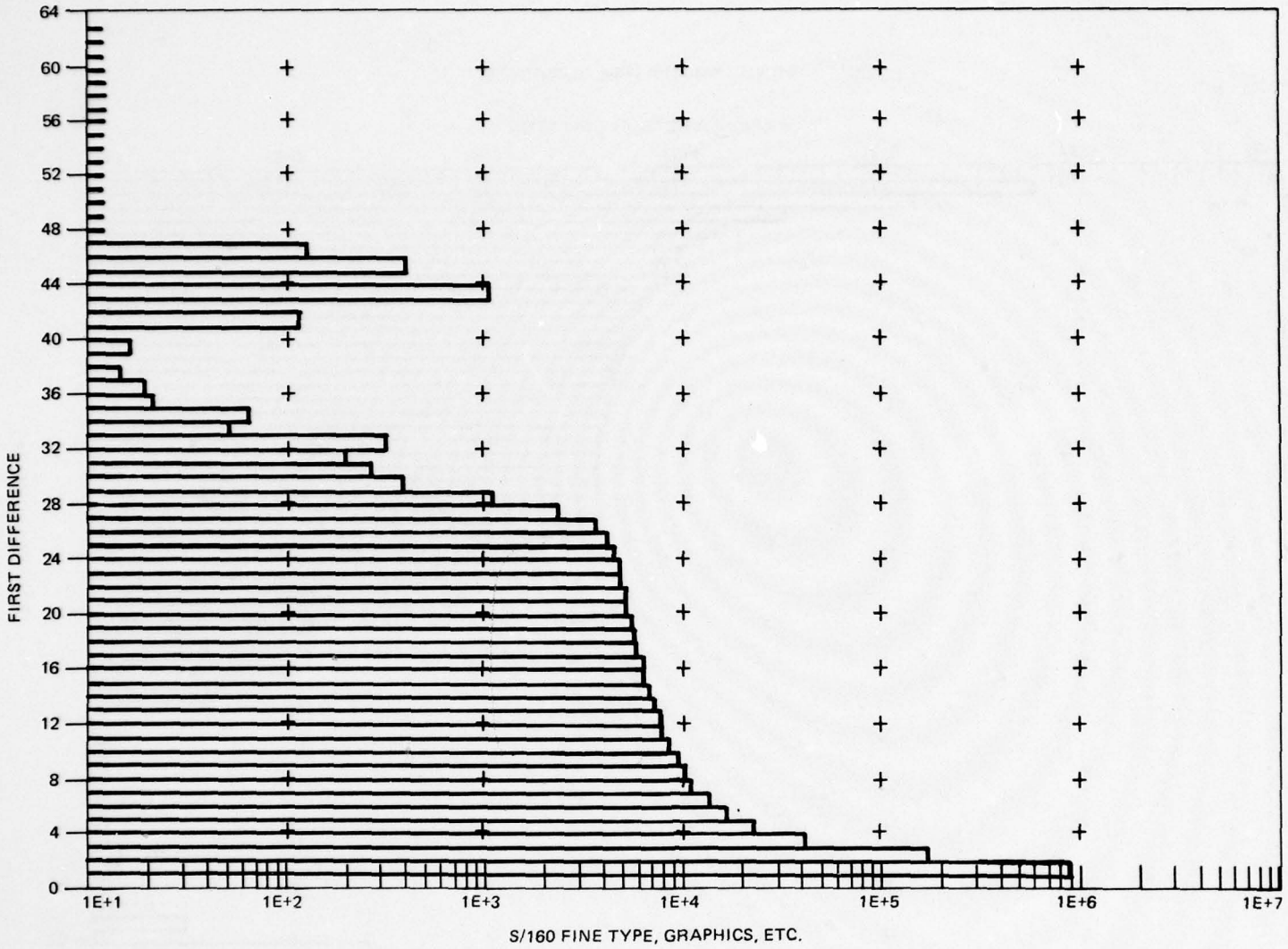


Figure B31. First difference statistics, 160 by 160.

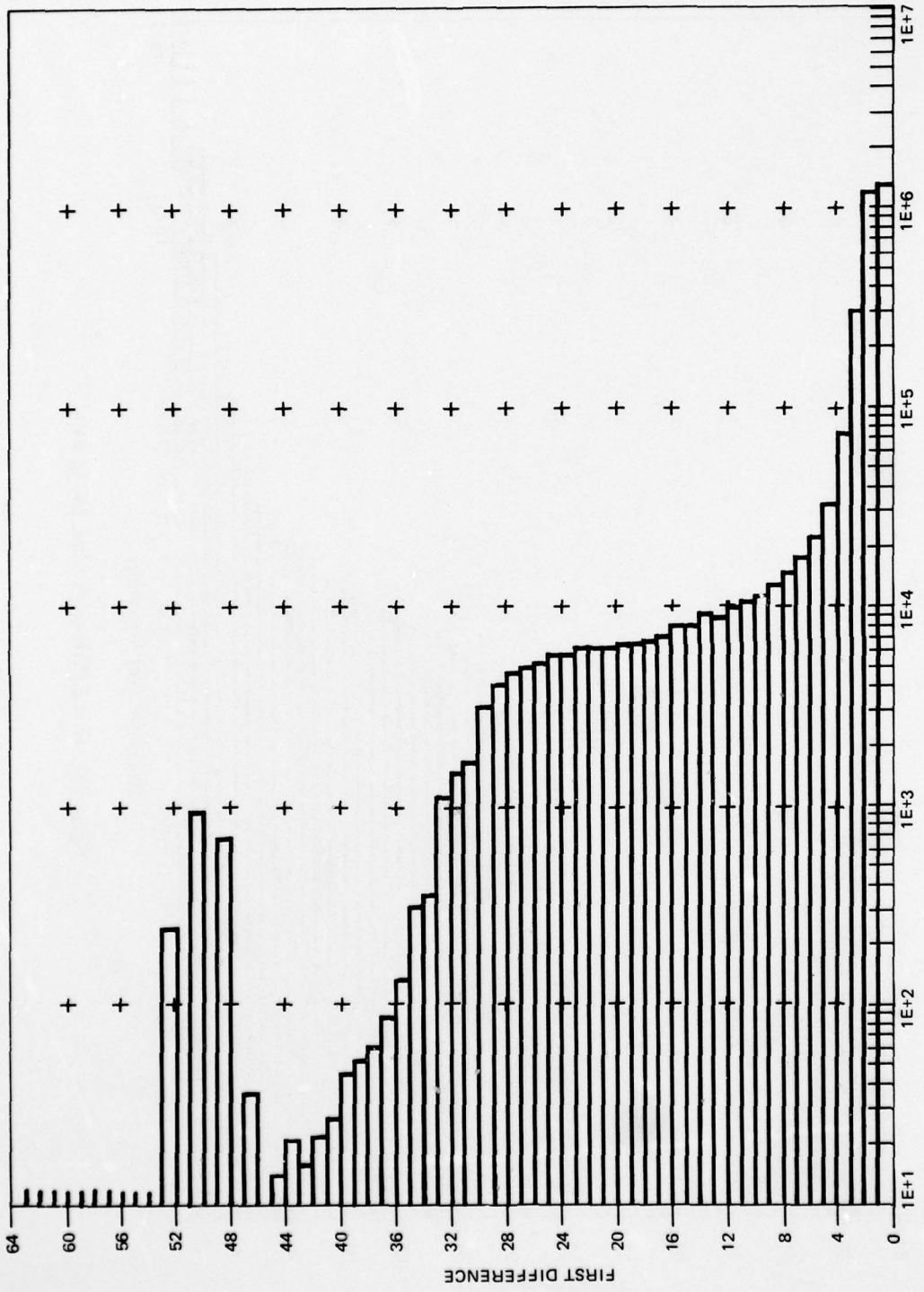


Figure B32. First difference statistics, 200 by 200.

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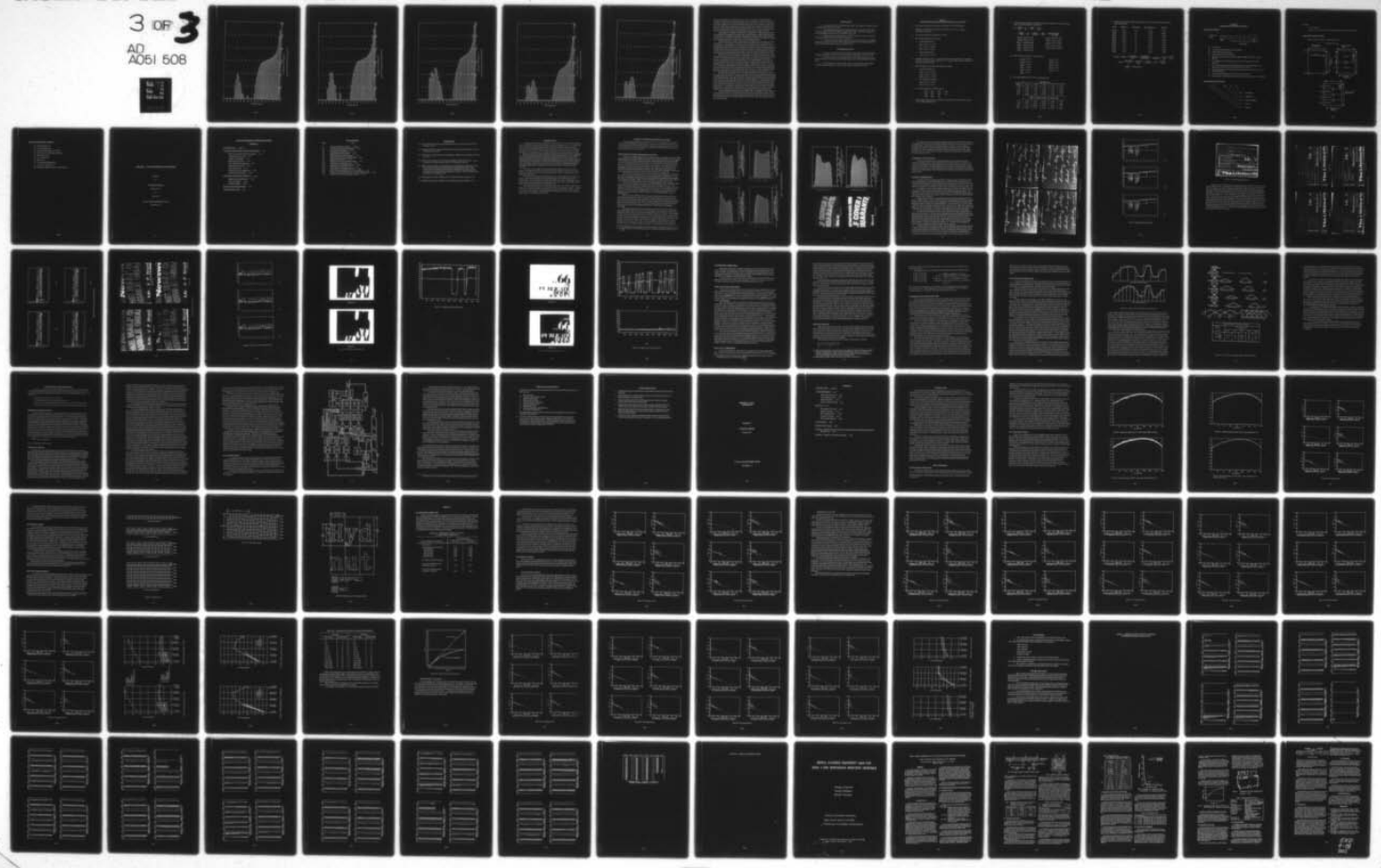


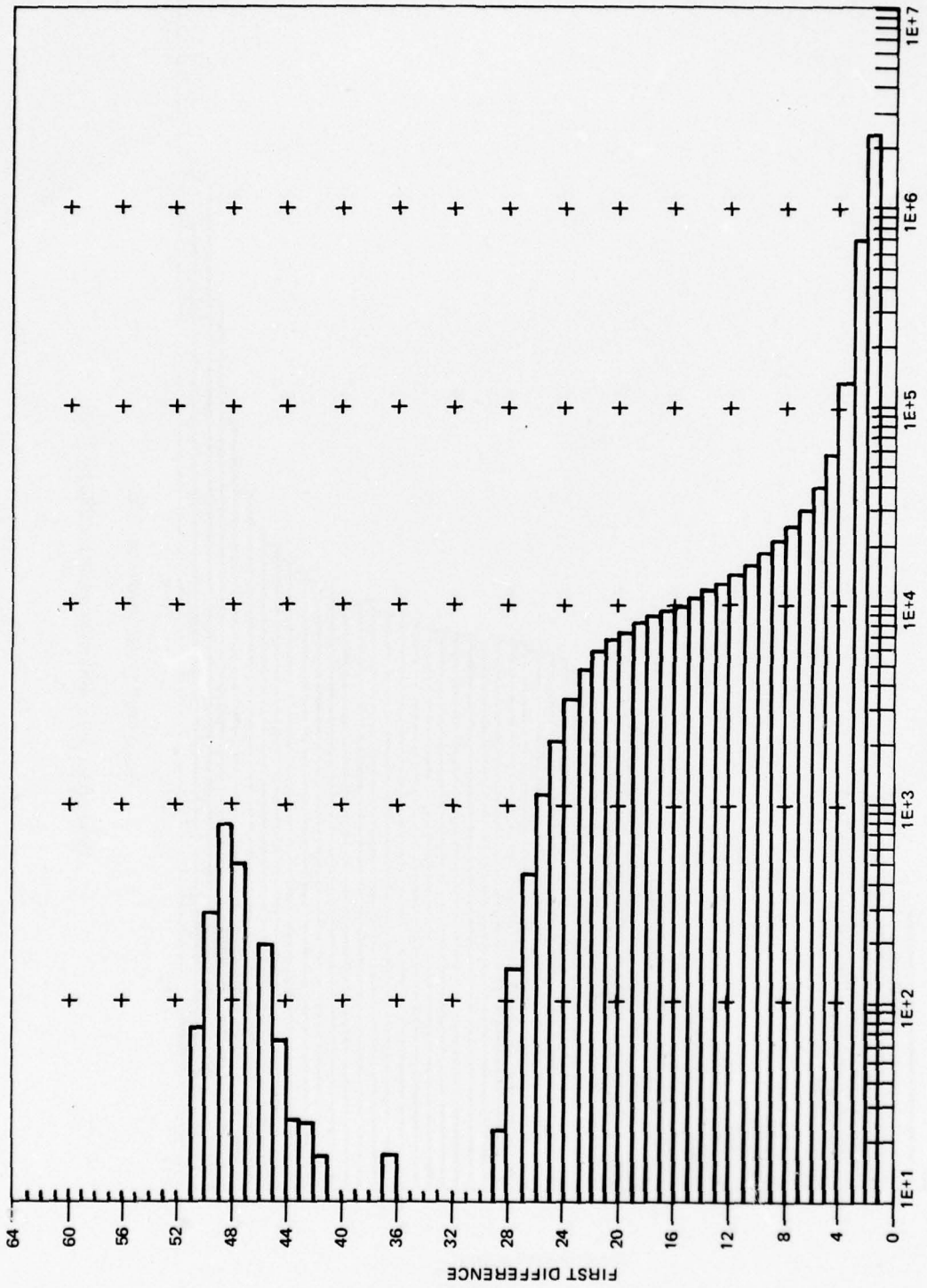


Figure B33. First difference statistics, 240 by 240.

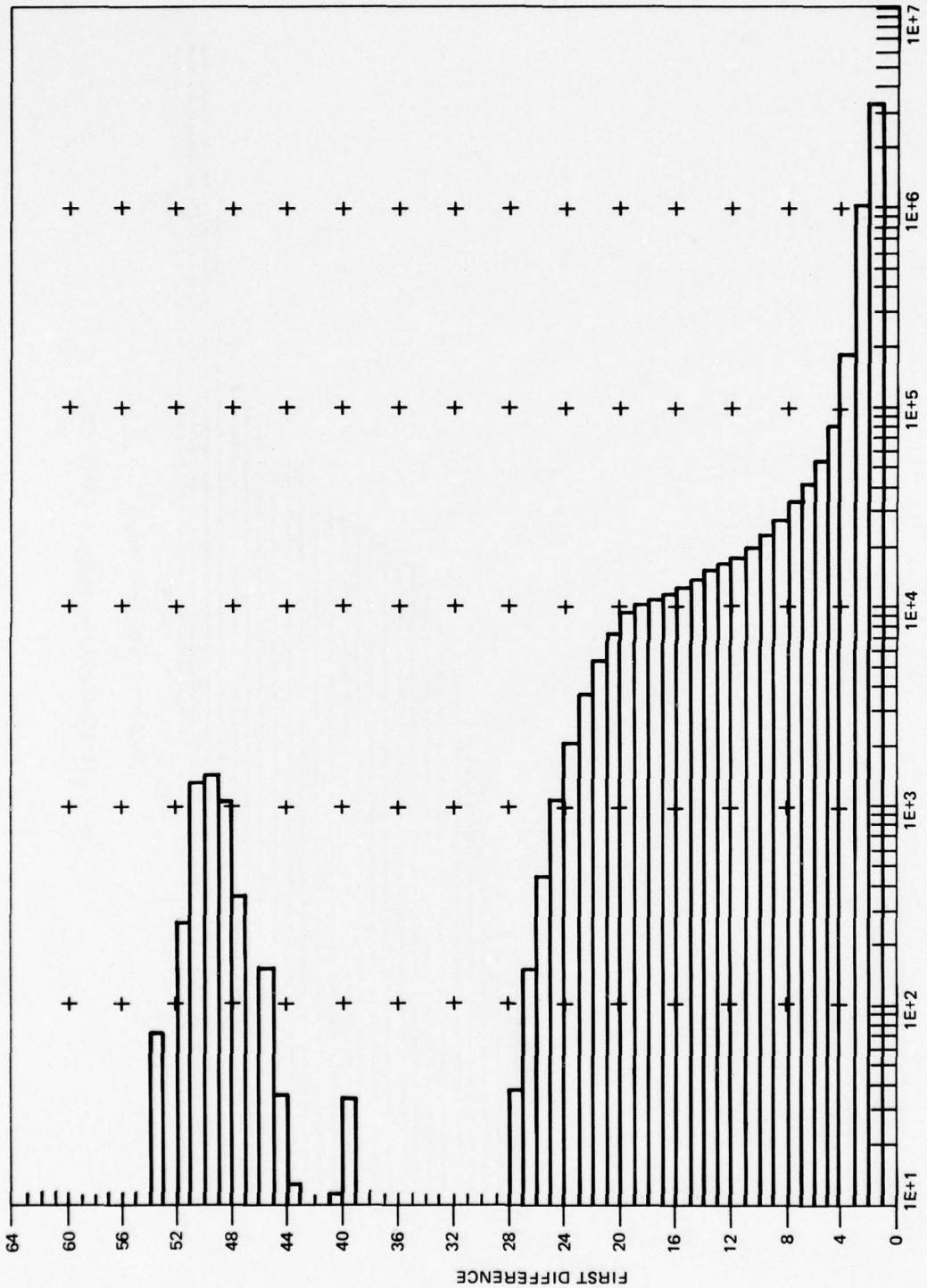


Figure B34. First difference statistics, 300 by 300.

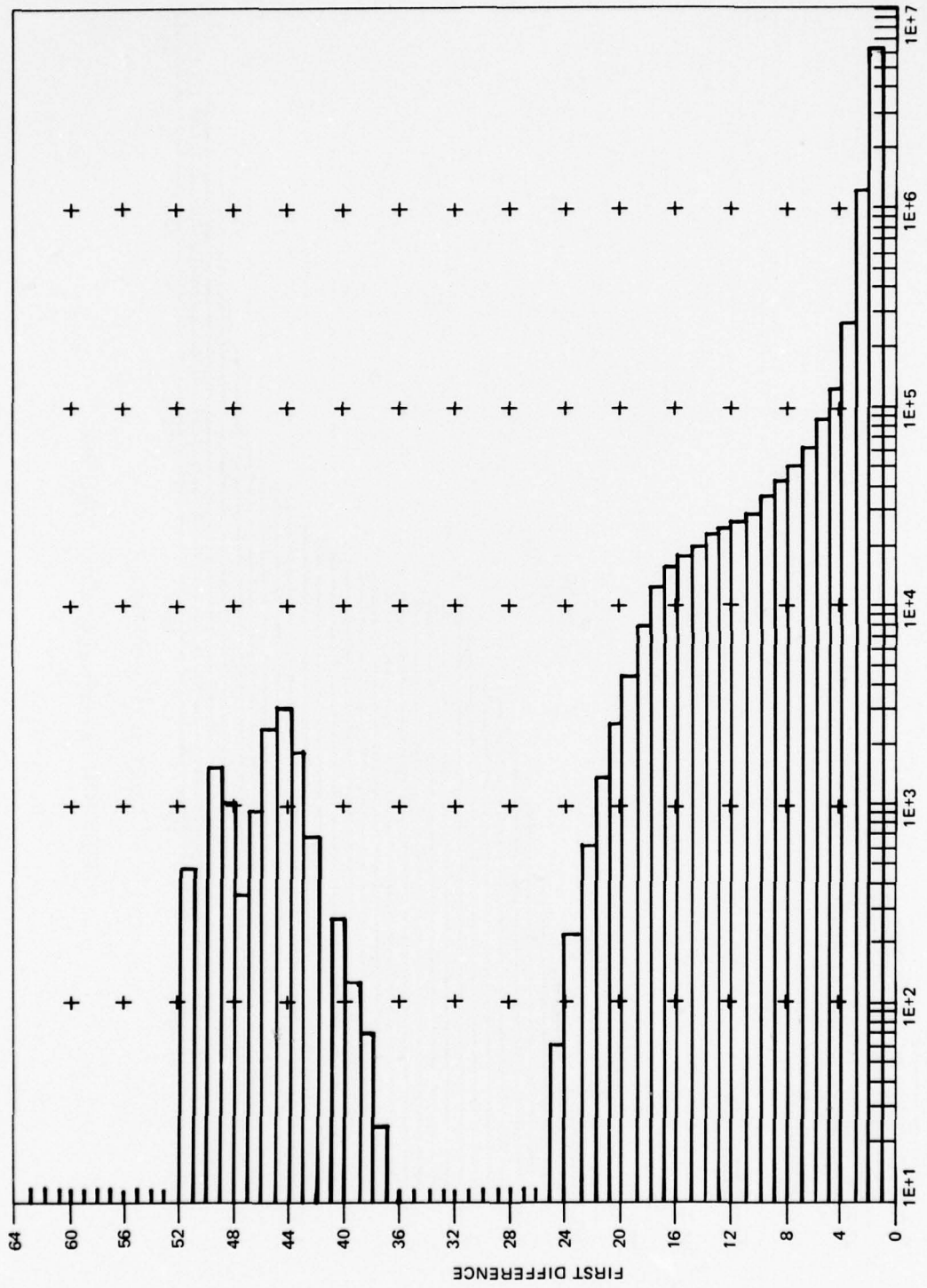


Figure B35. First difference statistics, 400 by 400.

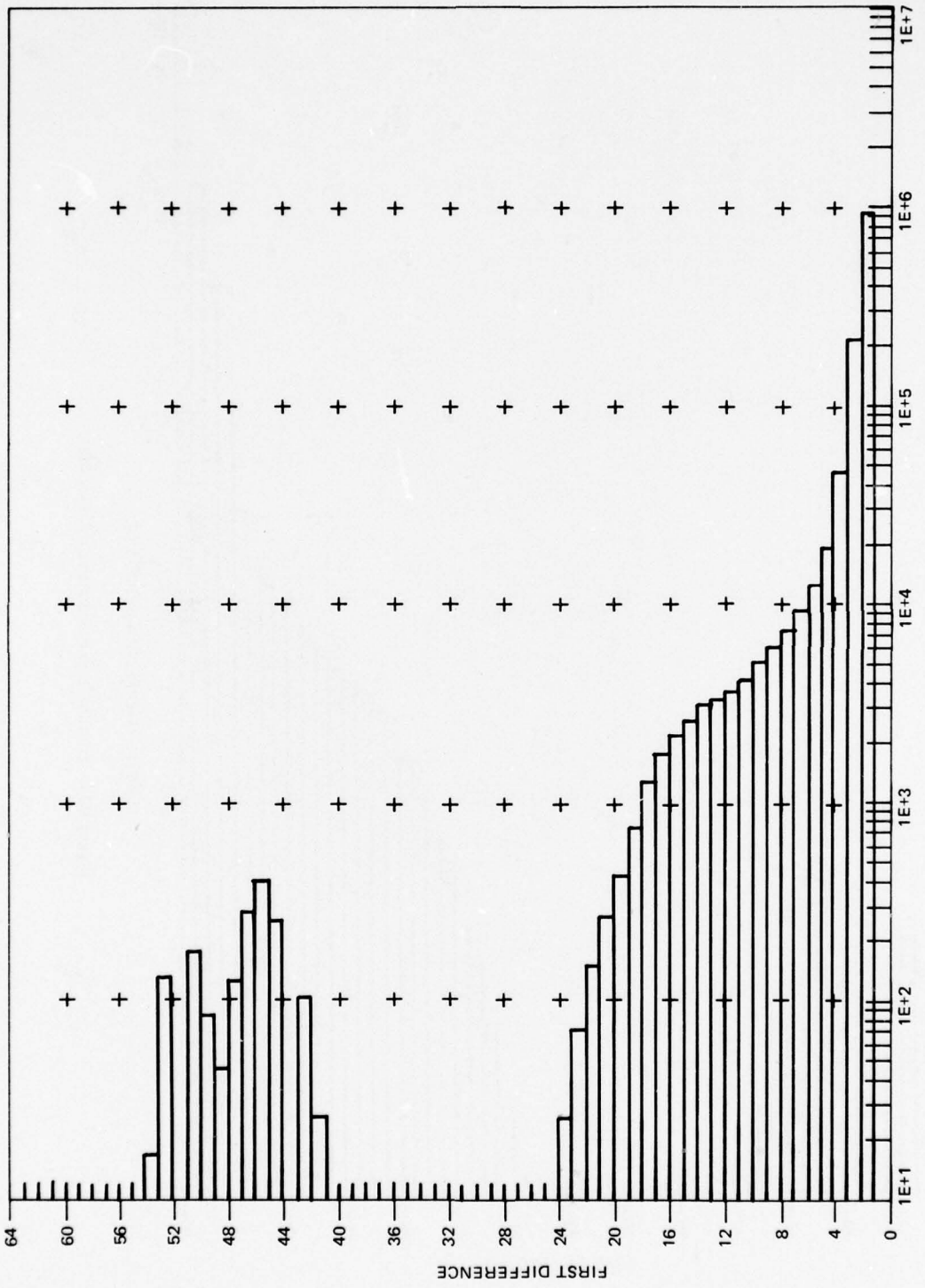


Figure B36. First difference statistics, 480 by 480.

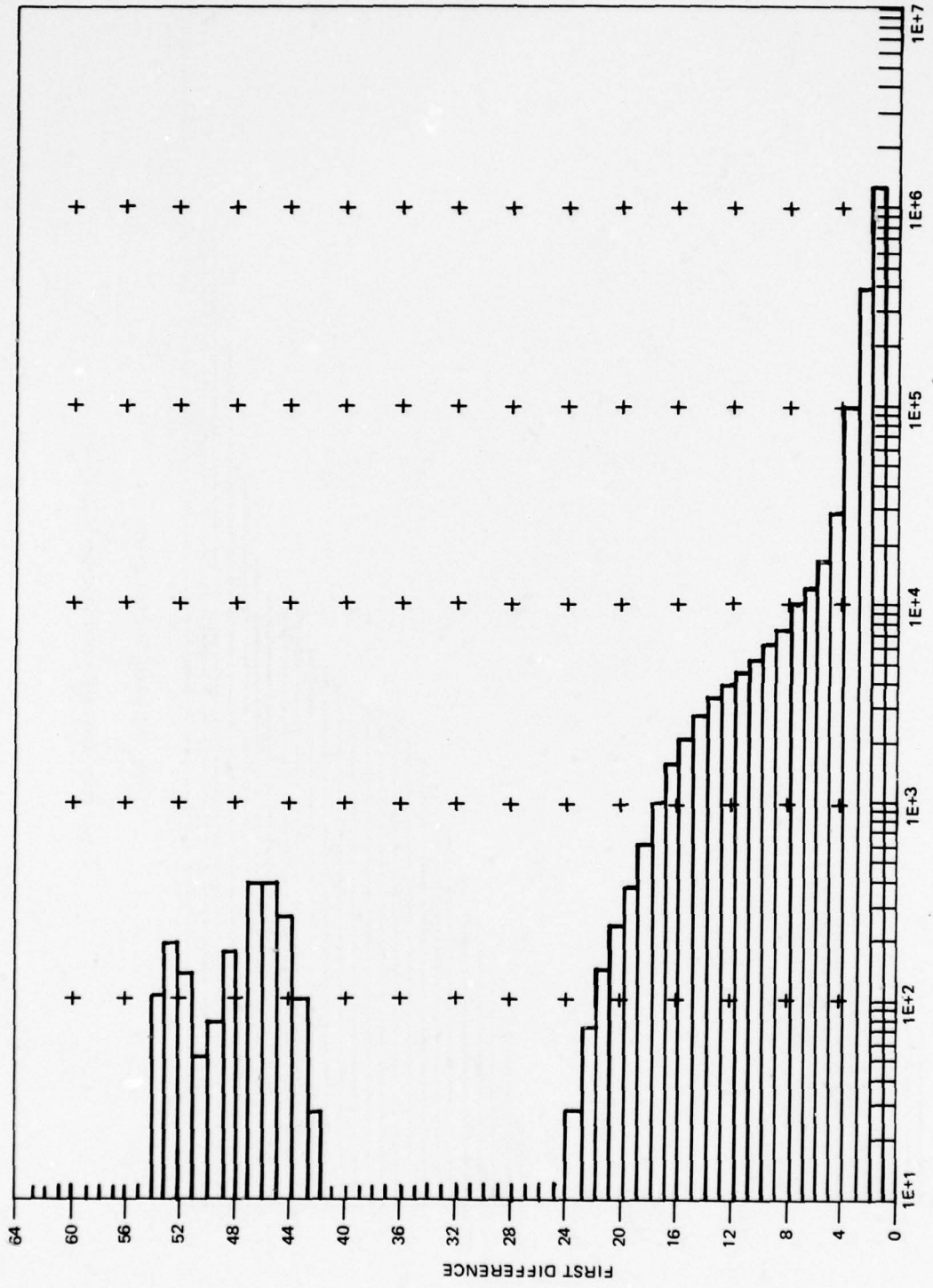


Figure B37. First difference statistics, 600 by 600.

43, then the absolute value of the difference 27–43 = 16 would be recognized and the storage bin containing the count of the number of times the difference was 16 would be incremented. This process is continued throughout the entire image. Exactly the same number of first differences is obtained as there were pels acquired. A special case is used for the difference as the imager acquires the first pel on the page. Since there is no valid previous value to compare to, the first pel value is subtracted from zero. In other words, there exists one value per line which represents the first large step up onto the imaged document.

Figure B30 is a histogram of FDS taken at a resolution of 120 by 120 pels per inch. At the bottom of the figure, the histogram bar running from left to right indicates that there are approximately 480 000 pels which provided the same reflection density, after illumination correction, as at least one adjacent pel. The figure also shows about 570 000 pels which have a brightness difference of only one level from a neighboring pel.

From differences 2 through 5 the histogram bar lengths shorten by about 1½ orders of magnitude. From differences 6 through 27 only small decreases in the quantities occur. Almost all the remaining differences are included in the range between 28 and 39. The remaining differences at the top of the histogram are the values of the initial pel brightness first encountered on each line whose values are subtracted from zero. When scanning at 120 by 120 pels per inch, there are 1320 lines per page. The tabular numerical data from which this histogram is made indicate that the sum of these artifact occurrences equals exactly 1320.

Figure B31 is an FDS histogram for data scanned at 160 by 160 pels per inch. There were more pels acquired at this resolution (2 393 600 vs 1 346 400) than at 120 by 120 pels per inch. Consequently, the values of first differences were in general somewhat higher. A change in resolution also affects the general shape of the FDS histograms. There are two reasons for this change. As the scan density increases, the displacement between adjacent samples decreases. In this series of samples, the range of displacements varies in a 5:1 ratio from 120-by-120- to 600-by-600-pel-per-inch sampling. Given a linear variation of brightness per unit of displacement on the copy material, the values of first differences should be quite different at the extremes of scanning densities used in this test. The above statement holds true if the modulation transfer function of the optics and imager is perfect (MTF = 1.0).

Because of the complexity of the interaction of the MTF, the frequency function of the image data in the direction of image scan, and the effects of quantizing the acquired data at various spatial frequencies, it is not possible to present a formal analysis of the relationships of the FDS at this time. The MTF is known to be approximately 0.67 at the Nyquist spatial frequency limit of the imaging device (38.5 line pairs per millimetre). The general waveform of the image data in the direction of imager scan can be defined as mostly in the high state with occasional band-limited excursions to a low state as portions of inked areas are crossed during the scan. It is planned to perform some simpler tests in the future with a few lines of copy having a controlled set of spatial frequencies. From this test, it is felt that the effects of MTF can be isolated from the effects of scanning density of typical printed material.

The remaining FDS histograms shown in figures B31 through B37 do show a decrease in large brightness differences with increasing spatial frequency of sampling. When actual percentages of total pels are calculated, the results show that 87.88%, 92.19%, and 93.53% of the first differences are less than three brightness levels for the 120, 300, and 600 resolution samples, respectively.

CONCLUSIONS

1. As expected, there is considerable improvement in the quality of images acquired as the spatial scan density is increased.

2. Thresholded images acquired at 200 by 200 pels per inch appear to be unsatisfactory to reproduce 5-point schoolbook (English News?) type. This resolution appears to be only marginally adequate for 5-point boldface Gothic type.

3. Images printed with full 6-bit grey scales are much easier to read and interpret, but should be printed with as much contrast as possible.

4. A scanning density of 200 by 200 pels per inch either grey scale or thresholded appears to be adequate for business letter typing, and lead pencil or ball point handwriting if the thresholds and dynamic ranges are carefully chosen.

FUTURE NOSC PLANS

1. Continue to study the effect of resolution of acquisition versus interpretability of images, particularly continuous-tone images, during the data capture studies in FY78.

2. Improve the interface between the ICAS and the NOSC laser printer facility. Images already have been printed with full 64-level grey scale on this equipment from ICAS tapes.

3. Closely monitor the RCA, Camden, study on relative address coding (RAC), smoothing, and interpolation as it affects image quality and required resolution.

ANNEX A:
VARIABLE RESOLUTION TEST, DRUM SPEED CALCULATIONS

1. Frame-store memory and tape transport cycle time, T_1 = 50 milliseconds.

2. Allowance for variation in drum speed, 2:1 then $T_2 = 2\,T_1 \geqslant T_1 + E_{MAX}$ = 100 milliseconds per line.

3. The low-speed drive motor speed is 0.5 rev/min.

4. The pulleys available for this shaft are:

   a. A triple with diameters:

      1.00″ + 0.137″ = 1.137″
      0.75″ + 0.137″ = 0.887″
      0.50″ + 0.137″ = 0.637″

   b. A single with diameter:

      1.40″ + 0.137″ = 1.537″

5. The above added value, 0.137″, is an empirical constant used with 0.1875″ neoprene belts which yields the effective diameter of a "V" groove pulley where the diameter of the groove bottom is known.

6. Pulleys available for the main drum shaft are as follows:

   a. A triple with diameters:

      4.250″ + 0.137″ = 4.387″
      4.061″ + 0.137″ = 4.198″
      3.840″ + 0.137″ = 3.977″

   b. Two singles with diameters:

      2.50″ + 0.137″ = 2.637″
      1.00″ + 0.137″ = 1.137″

7. The desired resolutions are (pels per inch):

2400	600	300	160
1200	480	240	120
800	400	200	

8 The left-hand column above is not needed for the RCA test, but these values may be useful for high-resolution tests.

9. The angular drum speed, W, is related to the drum circumference, C, the line storage time, T_2, and the resolution, R, required.

$$W = \frac{\text{LINE}}{T_2} \times \frac{1}{R} \times \frac{1\ \text{REV}}{C} \times \frac{60\ \text{s}}{\text{min}} =$$

$$= \frac{\text{LINE}}{0.100} \times \frac{1}{R} \times \frac{1\ \text{REV}}{13.653\ \text{in}} \times \frac{60\ \text{s}}{\text{min}} = \frac{43.945\ \text{LIN REV}}{\text{R IN MIN}}$$

W_{2400} = 0.0183 rev/min
W_{1200} = 0.0366 rev/min
W_{800} = 0.0550 rev/min
W_{600} = 0.0732 rev/min
W_{480} = 0.0815 rev/min
W_{400} = 0.1099 rev/min
W_{300} = 0.1465 rev/min
W_{240} = 0.1831 rev/min
W_{200} = 0.2197 rev/min
W_{160} = 0.2747 rev/min
W_{120} = 0.3662 rev/min

10. Pulley ratios required for 0.5 rev/min motors:

R_{2400} = 27.31:1
R_{1200} = 13.65:1
R_{800} = 9.10:1
R_{600} = 6.83:1
R_{480} = 5.46:1
R_{400} = 4.55:1
R_{300} = 3.41:1
R_{240} = 2.73:1
R_{200} = 2.28:1
R_{160} = 1.82:1
R_{120} = 1.37:1

11. The ratios obtained from the various combinations are:

	MAIN SHAFT				
DRIVE	4.387	4.198	3.977	2.637	1.137
1.537	2.854	2.731	2.587	1.716	0.740
1.137	3.858	3.692	3.498	2.319	1.000
0.887	4.945	4.733	4.484	2.973	1.282
0.637	6.886	6.590	6.243	4.140	1.785
	SAME AS ABOVE WITH 2.3:1 REDUCER				
1.537	6.564	6.281	5.950	3.947	1.702
1.137	8.873	8.491	8.045	5.337	2.300
0.887	11.373	10.886	10.313	6.840	2.949
0.637	15.838	15.157	14.359	9.522	4.105

12. All angular velocities (or slightly slower values) can be obtained by using the following pulley combinations:

RATE	DRIVE, in	REDUCER	MAIN SHAFT, in	LINES/s
W_{1200}	0.637	yes	4.437	8.522
W_{800}	0.887	yes	4.198	8.362
W_{600}	1.137	yes	3.977	8.486
W_{480}	1.537	yes	3.977	9.177
W_{400}	0.887	no	4.198	9.616
W_{300}	1.137	no	3.977	9.754
W_{240}	1.537	no	4.198	9.997
W_{200}	1.537	no	3.977	8.794
W_{160}	1.537	no	3.977	7.036
W_{120}	1.537	no	2.637	7.958

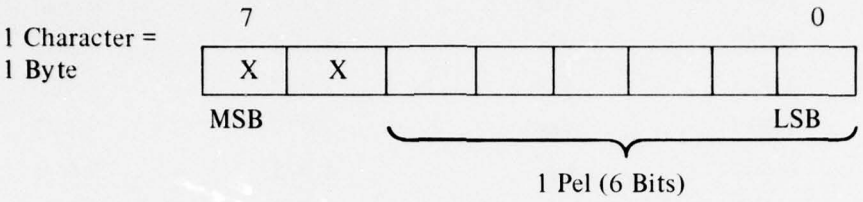
$$\text{LINES/s} = \text{RESOL} \times \frac{2\pi \text{ RADIUS}}{\text{REV}} \times \frac{\text{DIA DRIVE}}{\text{DIA MAIN}} \times \frac{1}{\text{REDUCER}} \times \frac{\text{min}}{60 \text{ s}} \times \frac{0.5 \text{ REV}}{\text{min}}$$

$$L_{600} = \frac{600 \text{ LINES}}{\text{in}} \times \frac{13.653 \text{ in}}{\text{REV}} \times \frac{1.137 \text{ in}}{3.977 \text{ in}} \times \frac{1}{2.3} \times \frac{0.5 \text{ REV}}{\text{min}}$$

$$\times \frac{\text{min}}{60 \text{ s}} = 8.486 \text{ LINES/s}$$

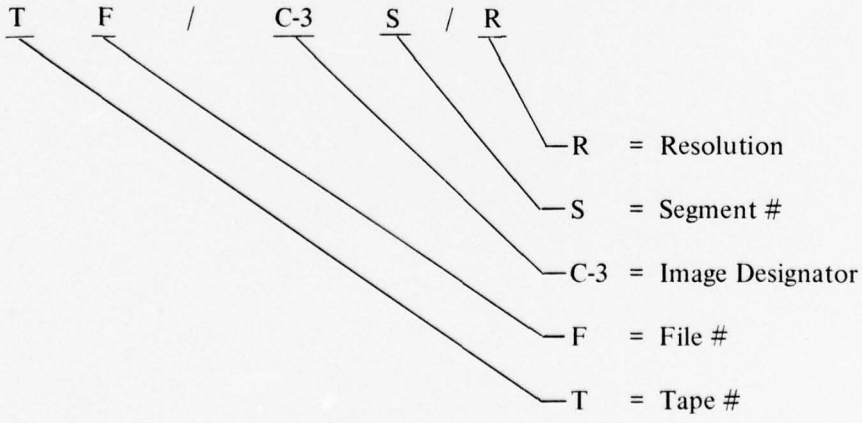
ANNEX B:
SUMMARY OF TEST SPECIFICATIONS

IMAGE TAPE FORMAT



- 1 line/record
- 1 file/captured image segment or half-segment
- Images illuminations corrected
- Images analyzed for PBS and FDS
- Images recorded on a Kennedy Model 9000 in "IBM Compatible" format at 800 CPI
- For resolutions of 200 points/inch and less, the scan line is in the 8½-in direction.
- For resolutions greater than 200 points/inch, the master image will be cut in halves, two each; (8½ by 5½ inch); and quarters, four each.
- For resolutions greater than 200 points/inch, the scan line will be in the 5½- or 2¾-inch direction.
- Tape file/image designation codes will be as shown below.
- For resolutions of 480 and 600 points/inch, place file mark for each half-segment.

IMAGE DESIGNATION CODE



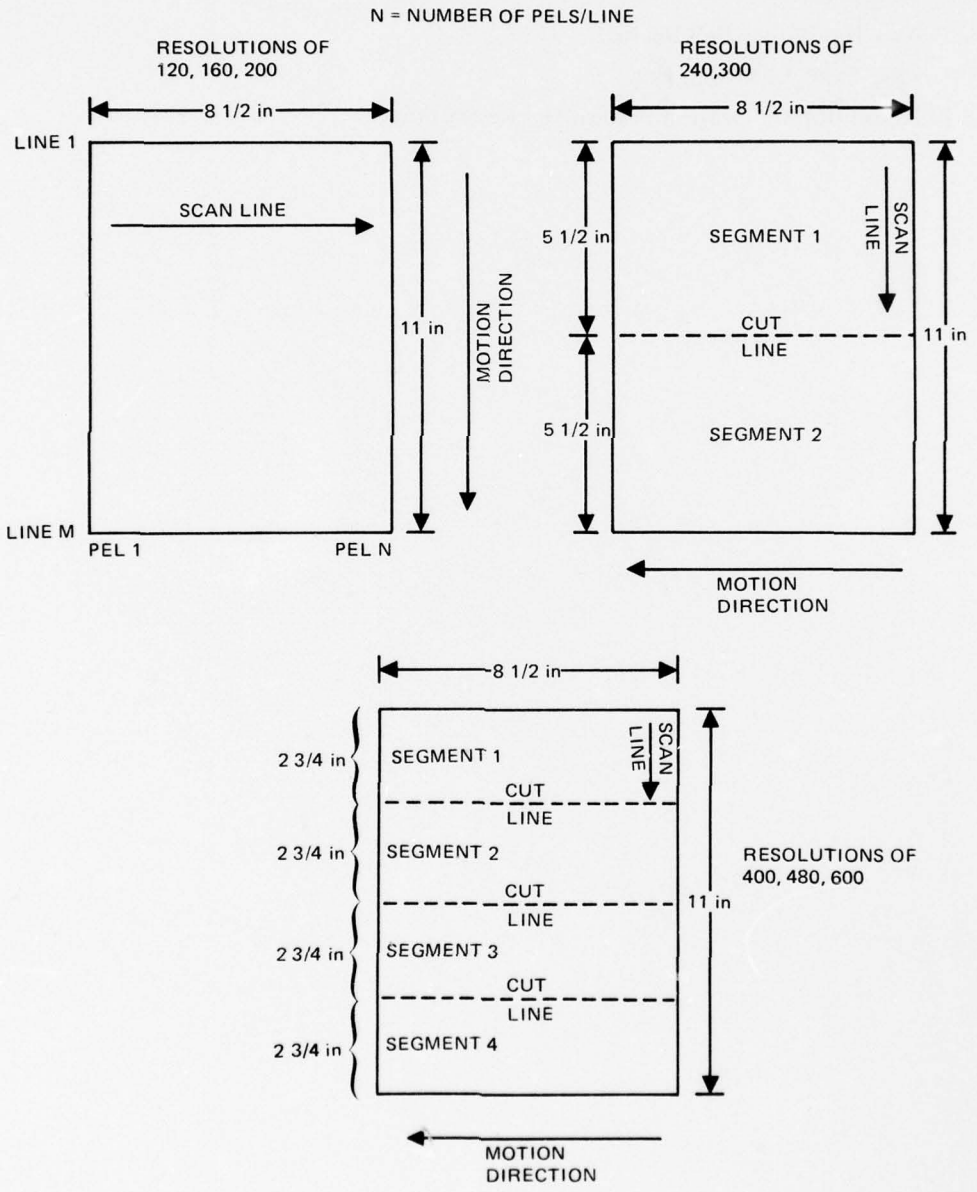
Example:

21, 3/T-2-4/480

Tape #21, File 3/RCA Form (Fourth Segment)/Scanned @ 480 points/inch

DOCUMENT SEGMENTATION

Images will be scanned in the following manner:



DESIGNATORS FOR RCA IMAGES

A-1 Flash Flash Flash $

A-2 Four Newspaper Ads

C-1 Letter from Senyo Electric to RCA

C-2 RCA Letter from Mr. Regan to Haynes

C-3 Handwritten Letter

T-1 D. C. Heath & Co.

T-2 RCA Form

T-3 New Hampshire Ball Bearing

S Fine Type, Graphics, Etc.

X-R Resolution Calibration Pattern (R=Resolution)

APPENDIX C: ADVANCED PRESTORAGE PROCESSING

Prepared

for

US POSTAL SERVICE

October 1977

by

Code 7323

NAVAL OCEAN SYSTEMS CENTER

San Diego, CA

ADVANCED PRESTORAGE PROCESSING REPORT

CONTENTS

ILLUSTRATIONS

REFERENCES

C1. First Annual Report, Advanced Mail Systems Scanner Technology, NELC TR 1965, October 22, 1975

C2. Second Annual Report, Advanced Mail Systems Scanner Technology, NELC TR 2020, October 1976, vol I & II

C3. Image Capture and Analysis System, Third Report, NOSC Code 7323 Summary Report, June 1977

C4. Real Time Correction of Acquisition Errors Applied To Solid State Scanners, a paper presented to the SPIE meeting, August 1977, San Diego, California

C5. Digital Facsimile Equipment, Quick-FAX Using a New Redundancy Reduction Technique, Yasuhiro Yamazaki, Yasushi Wakahara, and Hiroichi Teramura; R&D Laboratories of Kokusai Denshin Company, Ltd (KDD), Tokyo, Japan, a paper presented at the National Telecommunications Conference (NTC 76), Dallas, Texas, 29 November–1 December, 1976

C6. Data Compression Report, NOSC Code 7323 Summary Report, September 1977

C7. Image Resolution Report, NOSC Code 7323 Summary Report, September 1977

INTRODUCTION

The purpose of this report is threefold. The first objective is to review the prestorage processes which have been studied during the course of the program to date. A second objective is to initiate an attempt to integrate the most promising of these processes into the concept of a prototype USPS image scanning equipment. The final objective is to identify and prioritize areas of further subsystem study which may be required to improve marginal performance or provide data not yet available on which to make sound tradeoff decisions.

All the prestorage processing techniques discussed in this report have been accomplished by using software programs and microprocessor computational techniques on the digitized data. Processing done in this form is much slower than that required for real-time copy scanning at 20 pages per second. It should be emphasized that, for each algorithm discussed, a determination was made that a practical equivalent hardware subsystem can be designed which can perform each function in real time. In most cases the required 84-megapel-per-second throughput will be accomplished by using four parallel 21-megapel-per-second channels.

The review of the preprocessing studies undertaken thus far will be as concise as possible. Investigations which have previously been reported will be described only in the broadest terms with references to the documented source. Topics not previously covered will be described herein.

The systems integration tradeoffs will be given as careful consideration as possible at this time. Results from the Electronic Message Service System (EMSS) study by RCA, Camden, have not been completed or endorsed by USPS. The levels of complexity of a prototype image scanning equipment are highly dependent on the results of the EMSS study, as will be made obvious throughout the tradeoff discussion.

The identification of some areas requiring further study can be made at the outset of this report. The data base which now exists has come from relatively few "typical" examples of the types of copy material expected to become candidates for EMSS acquisition, processing, storage, and transmission. The USPS/NOSC FY78 statement of work already addresses major emphasis to expanding this data base.

CANDIDATE PRESTORAGE PROCESSES STUDIED

Nine distinctly different prestorage processes have been studied during the present and previous USPS/NOSC work agreements. In some cases, meaningful results could be obtained within a few days including software development and data acquisition. In other cases, in which a large number of samples are required to establish a significant statistical trend, the results are not yet conclusive.

WHITE LIGHT AND TRICOLOR PRESCAN ANALYSIS

The use of the Digital Image Analyzer (DIA) to produce pel brightness statistics (PBS) and first difference statistics (FDS) has been discussed in both references C1 and C2. Appendix D of reference C2 offers the best description of white light (420-620 nanometre) PBS. A copy of four histograms taken from reference C2 is repeated here. These are shown in figure C1. Both C1(a) and C1(b) are histograms of typed pages. The predominance of picture elements (pels) occurring at about brightness level 50 is due to the highly reflective bond paper on which the information is printed. The smaller hump on the bottom of these two histograms represents the toner or ink used to print the information. In these two cases, the frequency of occurrence of ink is about 4% that of the background.

The two lower histograms indicate a noticeably different distribution of pel brightness values. Figure C1(c) is an analysis of an outdoor photograph. The PBS curve is much more even on the right, indicating a more uniform distribution of brightness values found in the continuous-tone image. Figure C1(d) is a histogram of the IEEE facsimile chart, which contains both bilevel (black and white) and continuous-tone (photographic) images.

There are several important reasons for acquiring PBS data. First, the data contribute to the identification of bilevel or continuous-tone images. The PBS alone may not be sufficient to positively differentiate between bilevel and continuous-tone images, especially if there are small areas of continuous-tone image in the presence of a preponderance of bilevel data. It is expected that the PBS data plus some temporal data (line and character modulation sequences) will be required to produce a reasonable probability of correct differentiations.

The use of tricolor PBS will allow a selection of illumination for the main scanner which will provide maximum contrast. Figure C2 shows a segment of a Newsweek color advertisement which has been acquired and analyzed with filtered illumination. The image in figure C2(a) was acquired by using a Wratten 25 filter which has a spectral bandwidth from 580 to above 900 nanometres (nm). The corresponding histogram of figure C2(b) shows a relatively poor ratio of ink to background reflectance on the bottom to top humps, respectively.

The image of figure C2(c) was acquired by using a Wratten 47B blue filter having a spectral bandwidth from 390 to 470 nm. The third filter of the tricolor set, not shown, is the Wratten 58 green filter having a spectral bandwidth from 495 to 580 nm. The histogram of figure C2(d) is quite different from that of C2(b) in two respects. First, the ratio of the bottom to top (ink to background) humps of C2(d) is significantly larger than that of C2(b). Second, the ratio of pel brightness values is higher in figure C2(d) than in C2(b). This is an indication of two factors. More of the copy was recognized as black (dark) in the lower example. Also, the reflectance of the inks as acquired by the imager was lower when the blue filter was used causing the statistics to change as a result of the increasing contrast.

C1. First Annual Report, Advanced Mail Systems Scanner Technology, NELC TR 1965, October 22, 1975
C2. Second Annual Report, Advanced Mail Systems Scanner Technology, NELC TR 2020, October 1976, vol I & II

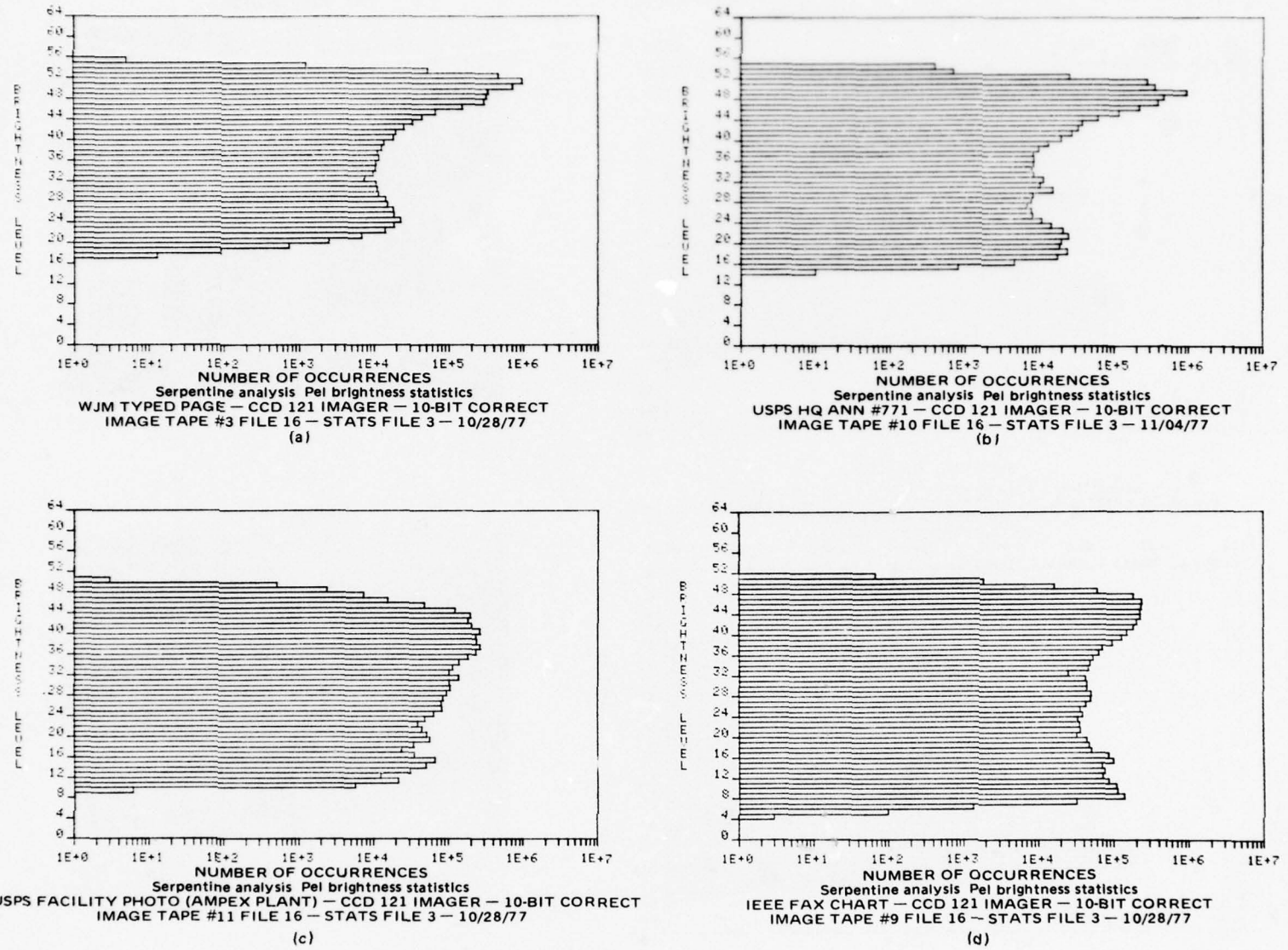
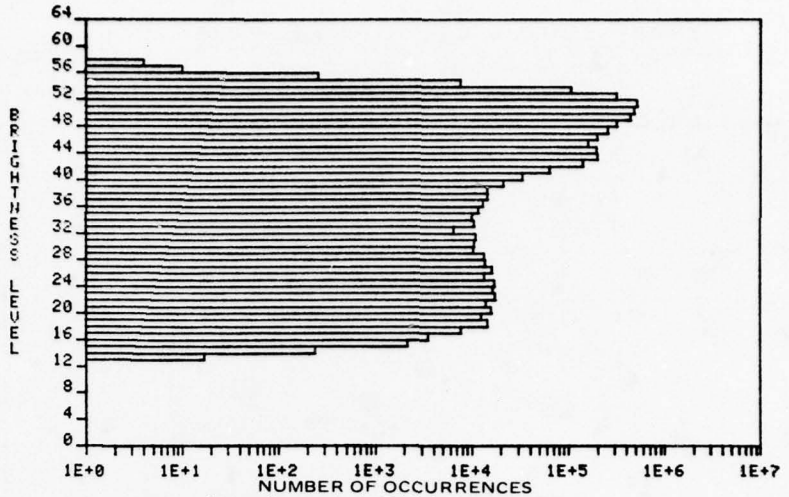


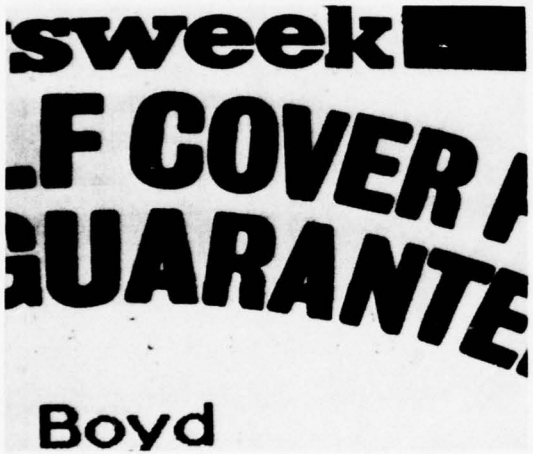
Figure C1. Typical pel brightness statistics.

RED FILTER (a)

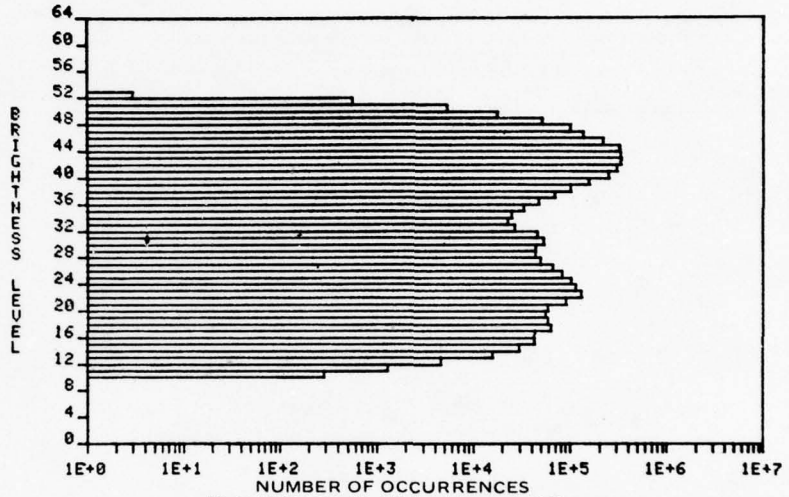


Serpentine analysis Pel brightness statistics
TRI-COLOR COPY — RED FILTER — CCD 121 IMAGER — 10-BIT CORRECT
IMAGE TAPE #14 FILE 16 — STATS FILE 3 — 11/04/77

RED HISTOGRAM (b)



BLUE FILTER (c)



Serpentine analysis Pel brightness statistics
TRI-COLOR COPY — BLUE FILTER — CCD 121 IMAGER — 10-BIT CORRECT
IMAGE TAPE #16 FILE 16 — STATS FILE 3 — 11/04/77

BLUE HISTOGRAM (d)

Figure C2. Color filtering contrast enhancement.

The histogram is also useful in determining the brightness level at which to establish a threshold. This is only true if relatively even illumination is provided across the document or if illumination compensation is used before analysis. In figure C1(a) the optimum threshold level for the bilevel image should be placed at about level 32 (the saddle point). In figure C1(b), whose original image contained a USPS logo, the threshold choice might be level 35 or level 25, depending on whether to include the middle hump as information or background, respectively.

AUTOMATIC GAIN AND LEVEL

The prescan histograms also provide information about an image which allows settings to be made for the control of gain and level during the main scan acquisition. An increase in gain widens the histogram distribution curve, and a level change can be used to provide an offset which centers the histogram in the range between levels 00 and 63. When properly set, the gain and level adjustments provide acquisitions exploiting the full brightness dynamic range of the system. The circuits for remote control of gain and level are described in reference C3.

ADAPTIVE THRESHOLDING

As mentioned previously in the discussion on image analysis, one method of establishing a threshold is to use the PBS histogram to determine the saddle point between the two predominant brightness level peaks and utilize this dividing value as the threshold. This concept only works well in equipments which contain illumination correction circuits or are otherwise compensated to provide flat response from copy materials of uniform reflectance.

By telephone contact with Fairchild Imaging Systems, Syosset, NY, NOSC received a description of a novel method of providing an analog adaptive threshold technique. The algorithm, as understood at that time, was programmed for the USPS/NOSC Image Capture and Analysis System (ICAS), and sample sections of images, both with and without illumination correction, were evaluated.

Figure C3(a) is a portion of a handwritten letter as scanned and digitized to 6 bits per pel. Figures C3(b), (c), and (d) show the resultant bilevel images produced by thresholding with various adjustments of the circuit parameters. Figure C4 shows actual plots of the image data on line 15, labeled P, and the threshold, T, as it tracks the data. In this example the first few dark lines (negative excursions of the P curve) have a contrast ratio of about 0.6 and easily cross the threshold. The dark line to the right of the plot, that only extends down to level 37, has a contrast ratio of 0.23 and consequently does not cross the threshold.

The next set of examples was made with a multicolor document, a photograph of which is shown in figure C5. This document was scanned with broadband illumination and digitized at 6 bits per pel. This image was thresholded with the same algorithm and the same set of parameters as the handwritten page. The area of interest in this group of photographs is near the bottom where the cursor runs through the bold typing. The type is red ink on a white background with the lines in black. For the red typing on the line profile plots in figure C7, the print contrast ratio is about 0.37. As seen in the photographs in figure C6, all but figure C6(d) exhibit a certain amount of tearing.

Another example of low print contrast ratio thresholding is shown in figures C8 and C9, figure C8(a) being the original 6-bit image. The line plotted in figure C9 is near the top of the image through the line of bold type. Figure C9 indicates that this point has a print contrast ratio of about 0.33, very close to the minimum requirement for thresholding.

C3. Image Capture and Analysis System, Third Report, NOSC Code 7323 Summary Report, June 1977

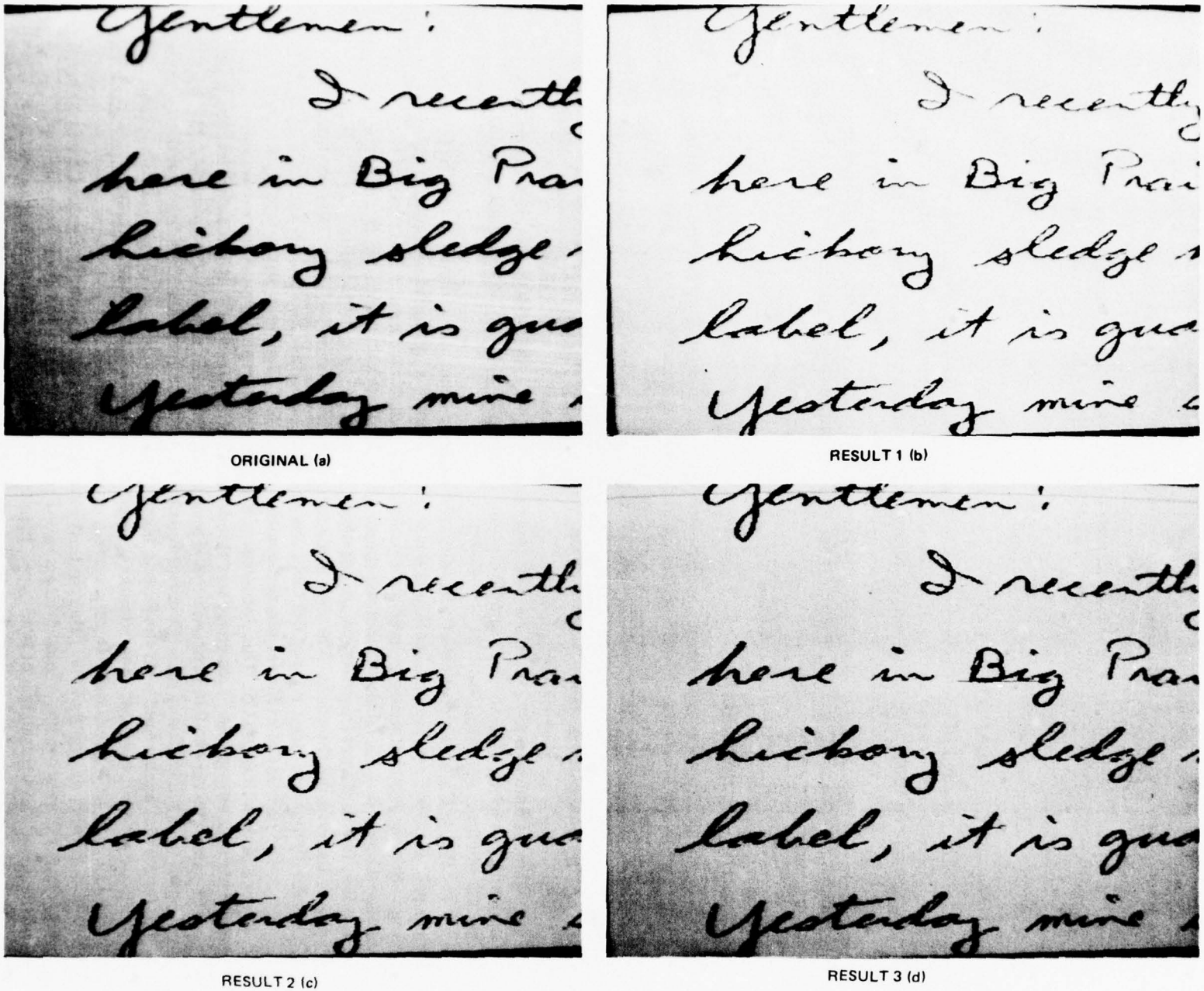
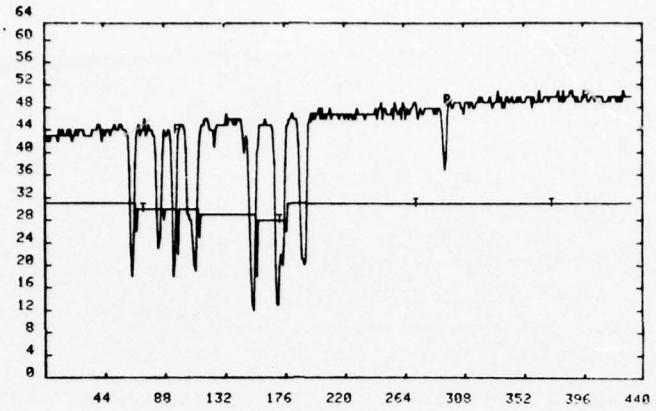
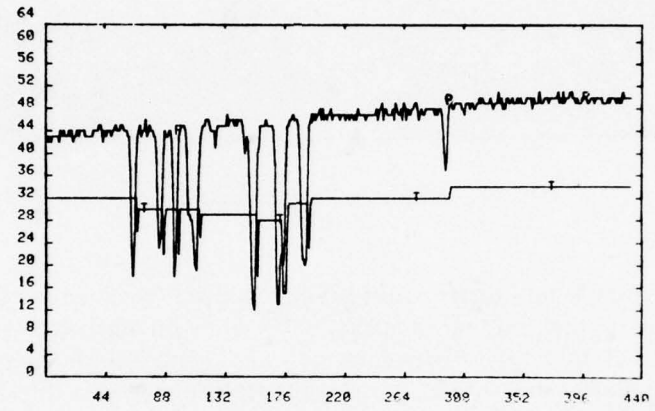


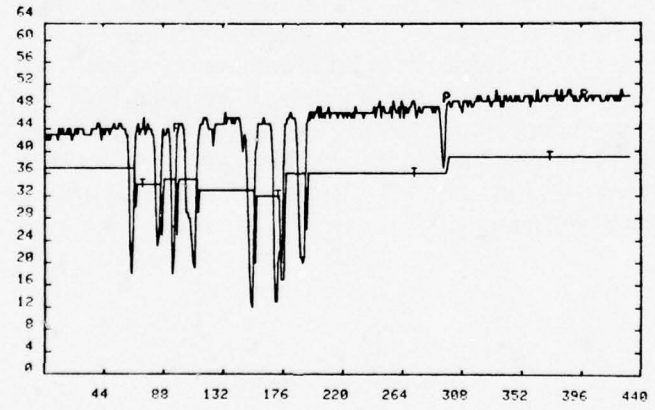
Figure C3. Thresholded handwriting.



(a)



(b)



(c)

Figure C4. Handwriting threshold profiles.

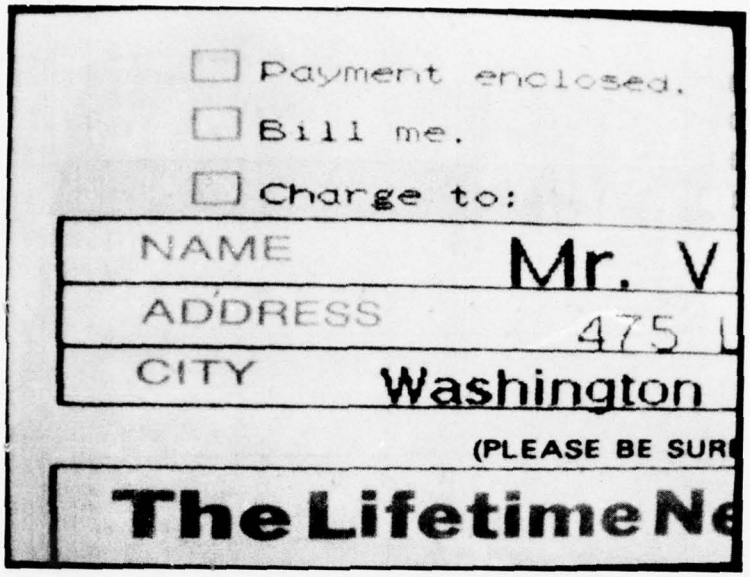
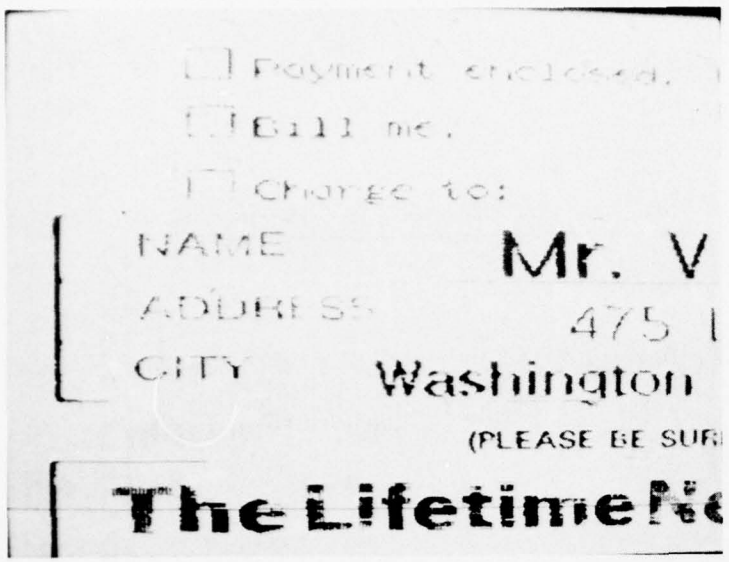
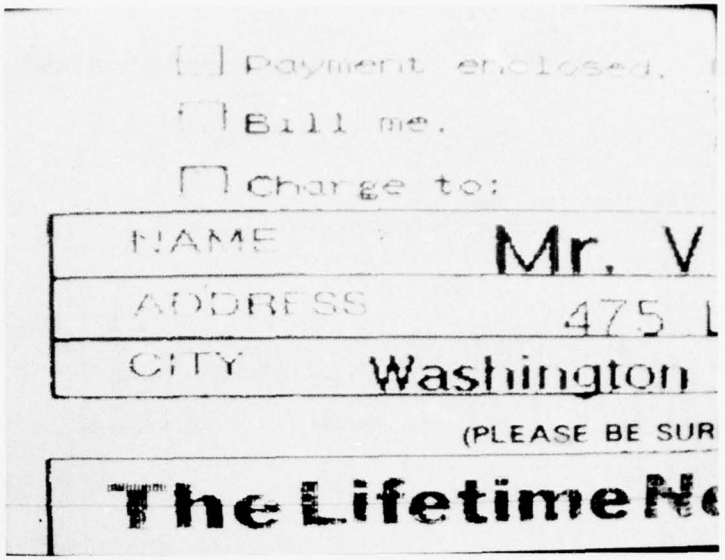


Figure C5. Original multicolor document.

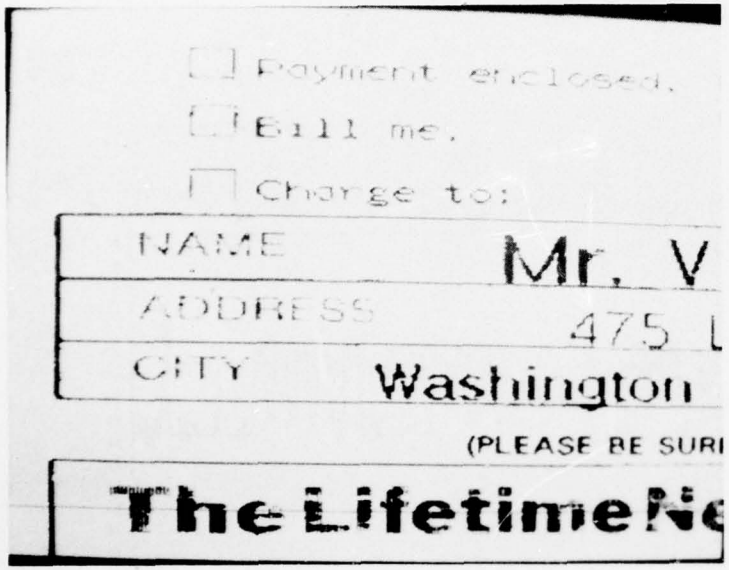
Two portions of a NOSC library acquisitions cover were scanned in order to demonstrate problems, if any, in thresholding an image that is white on black versus the typical black on white format of most typewritten information. Figure C10 shows a portion of this image which is predominately white. There is no problem with the thresholding algorithm here. Figure C11 shows a line profile to demonstrate this. The second portion of this is shown in figure C12. Note that figure C12(b) is shown inverted rather than white on black. Figure C13(a) shows a line profile through the printing toward the bottom of the image. The upper portion of the image, however, shows a potential problem which is that of scanning a large area of black information. At low image brightness levels the upper and lower thresholds are very close to the image brightness level, typically within one or two intensity levels. Thus, any minor fluctuations in the image data have a high likelihood of crossing the threshold. This is the reason for the salt-and-pepper effect in the upper portion of the photograph in figure C12(b). Figure C13(b) shows a line plot of the last line of the salt-and-pepper portion of the image.



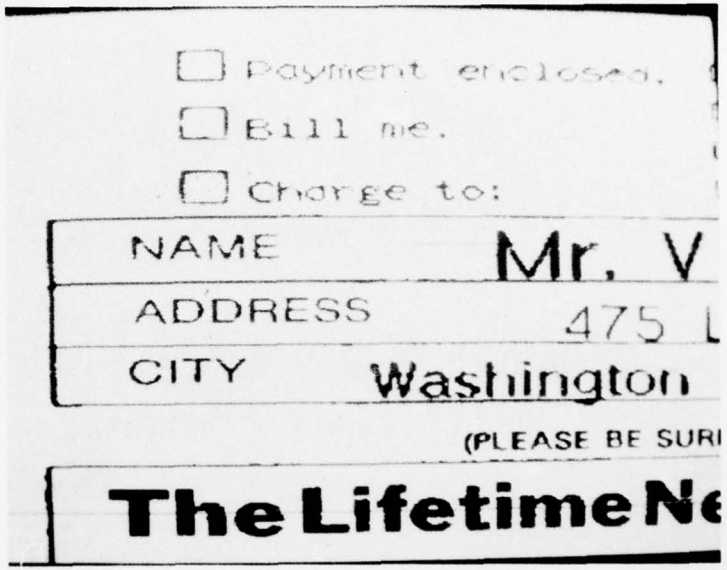
RESULT 1 (a)



RESULT 2 (b)

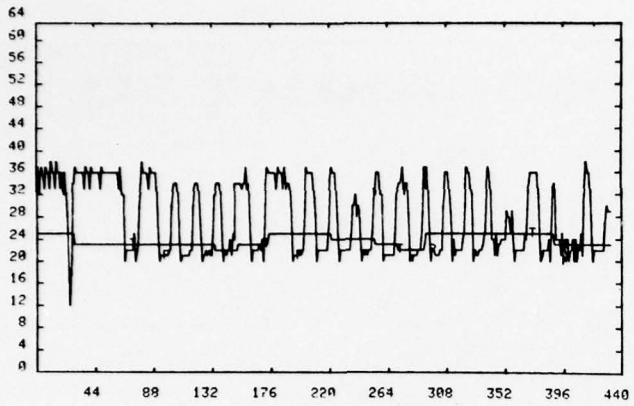


RESULT 3 (c)

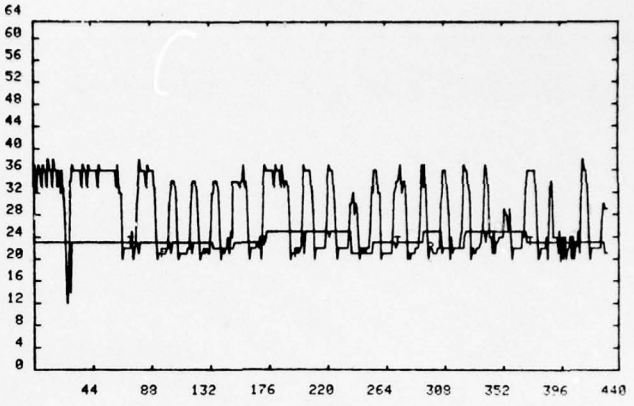


RESULT 4 (d)

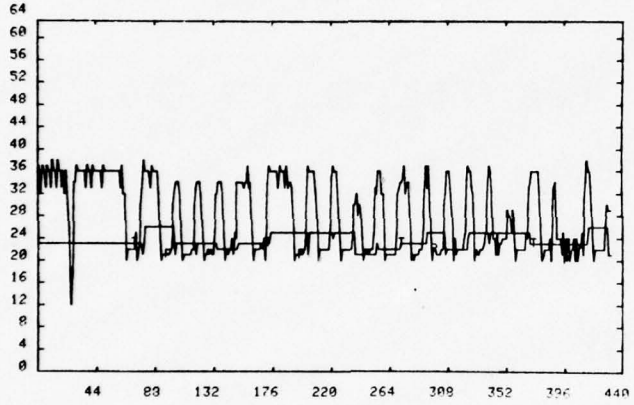
Figure C6. Thresholded multicolor document.



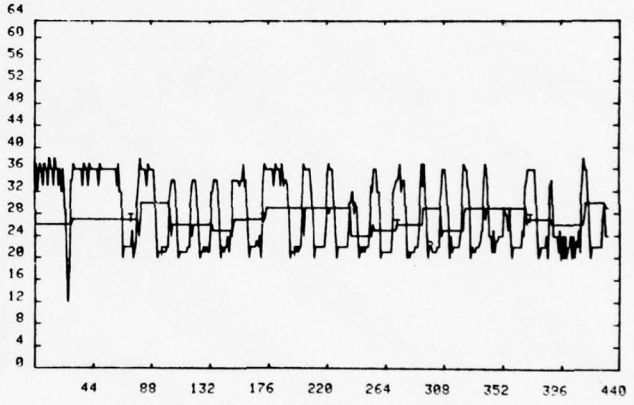
(a)



(b)

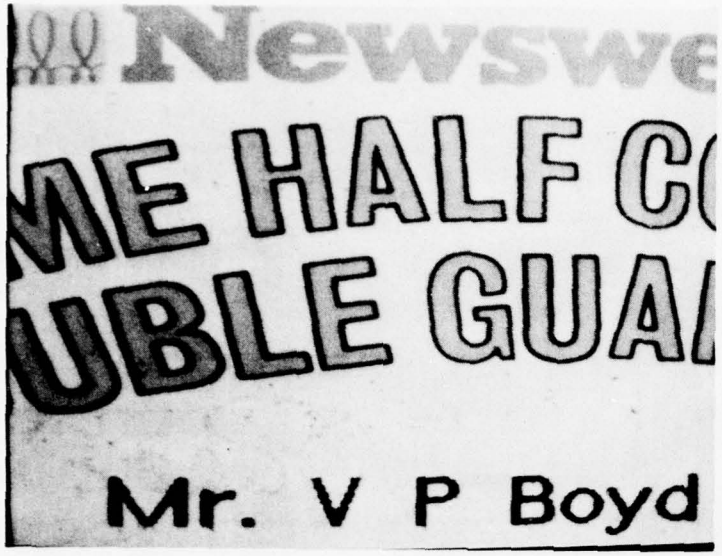


(c)

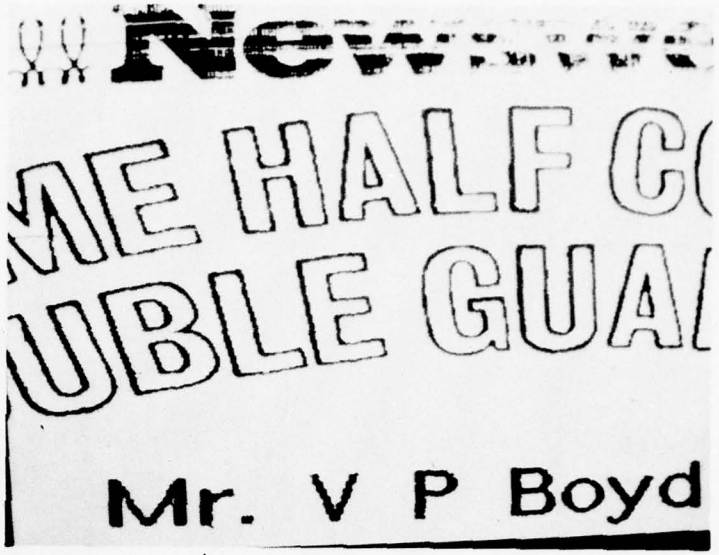


(d)

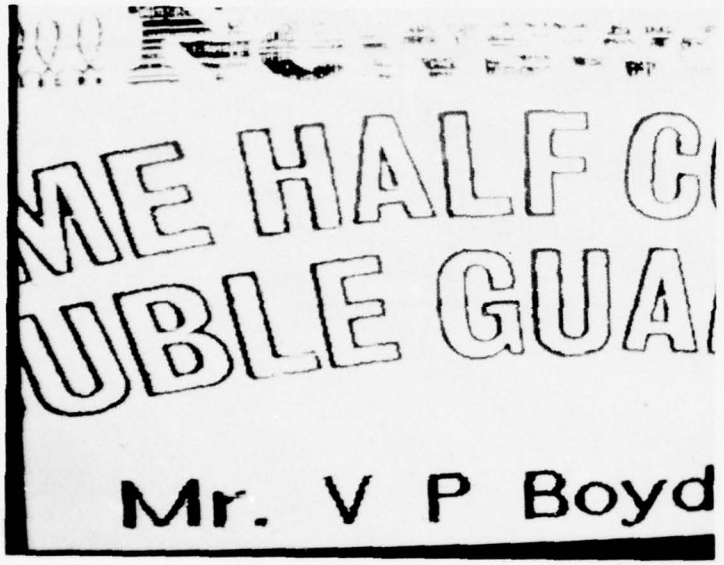
Figure C7. Multicolor document threshold profiles.



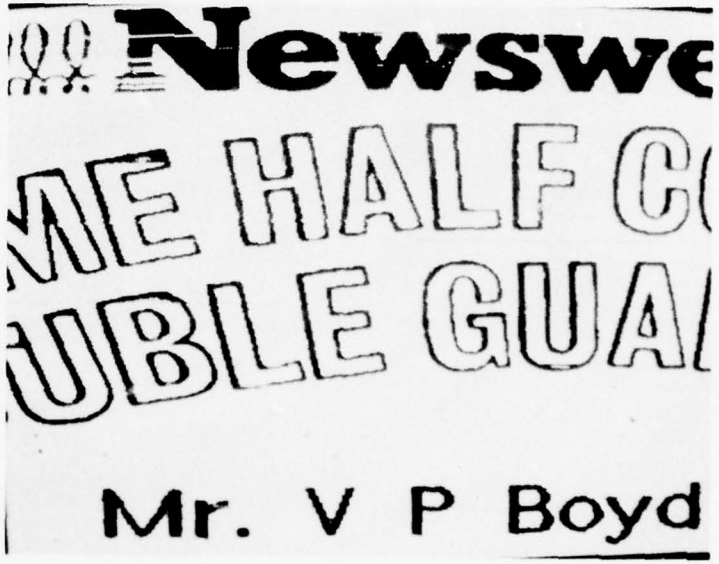
ORIGINAL (a)



RESULT 1 (b)

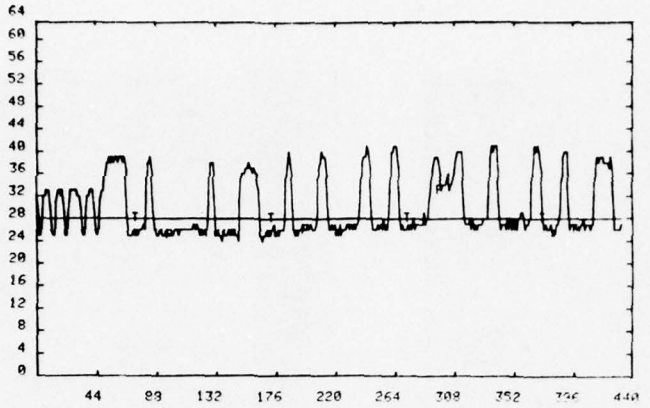


RESULT 2 (c)

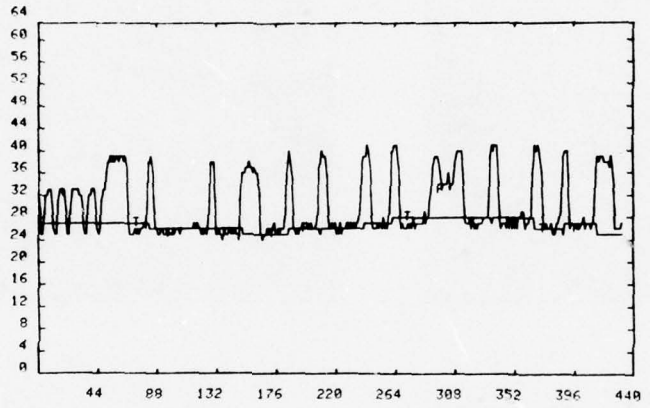


RESULT 3 (d)

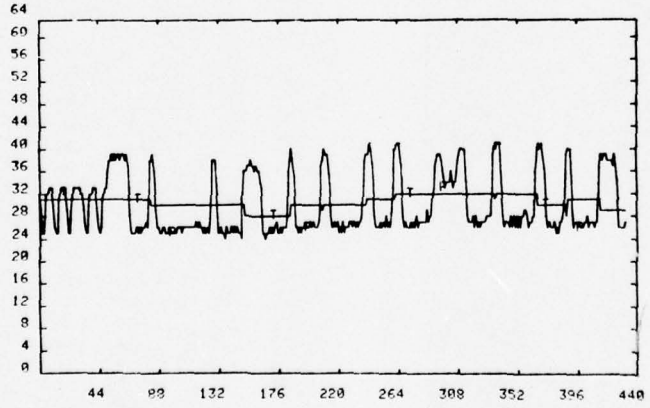
Figure C8. Multicolored document.



(a)



(b)



(c)

Figure C9. Multicolor document threshold profiles.

ORIGINAL (a)

RESULT (b)

Figure C10. NOSC library acquisitions cover.

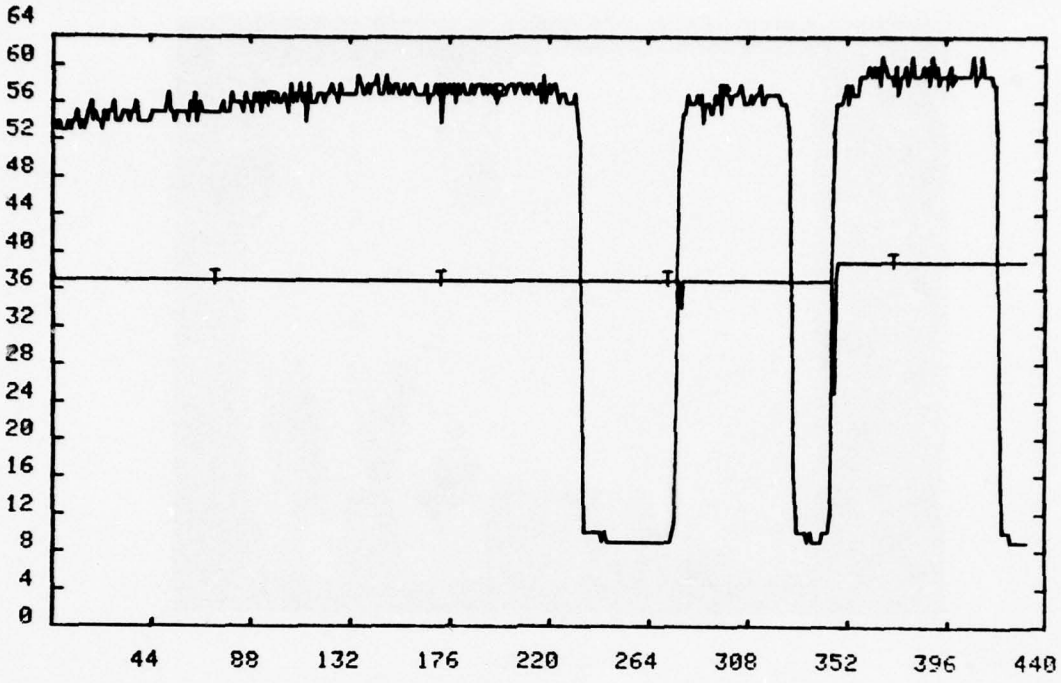
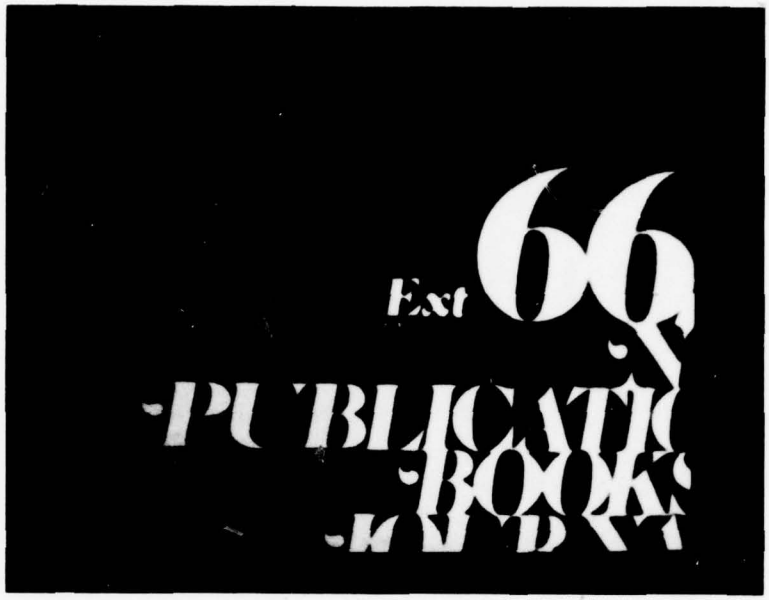
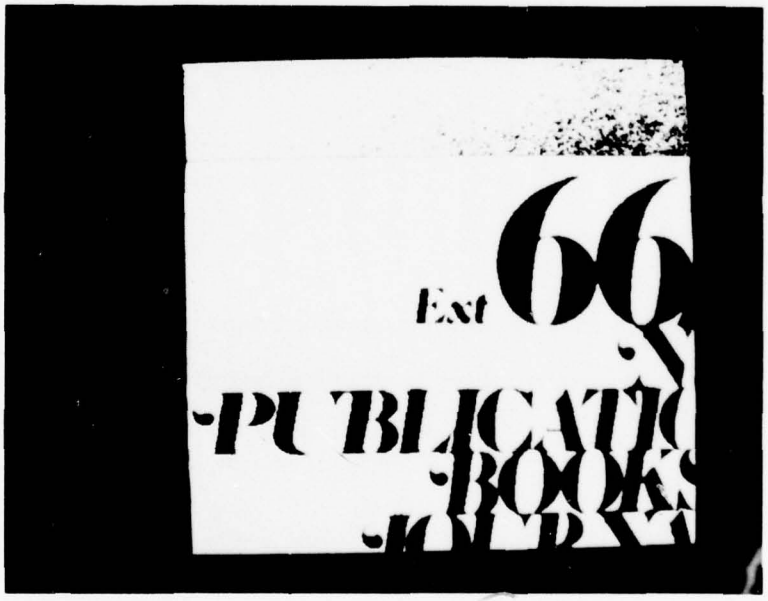


Figure C11. Acquisitions cover threshold profile.

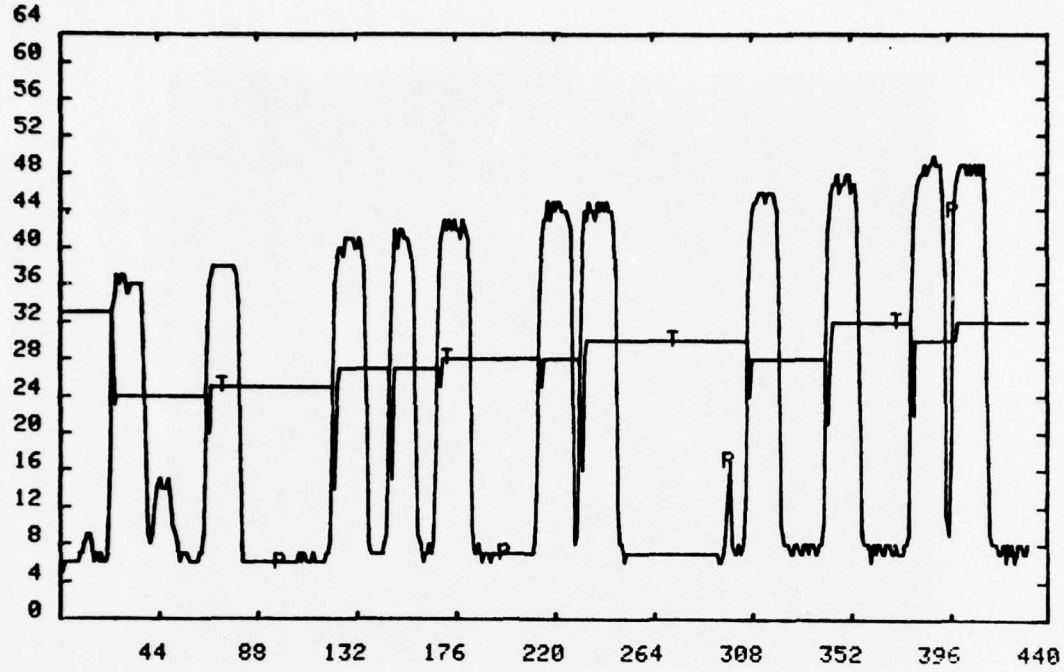


ORIGINAL (a)

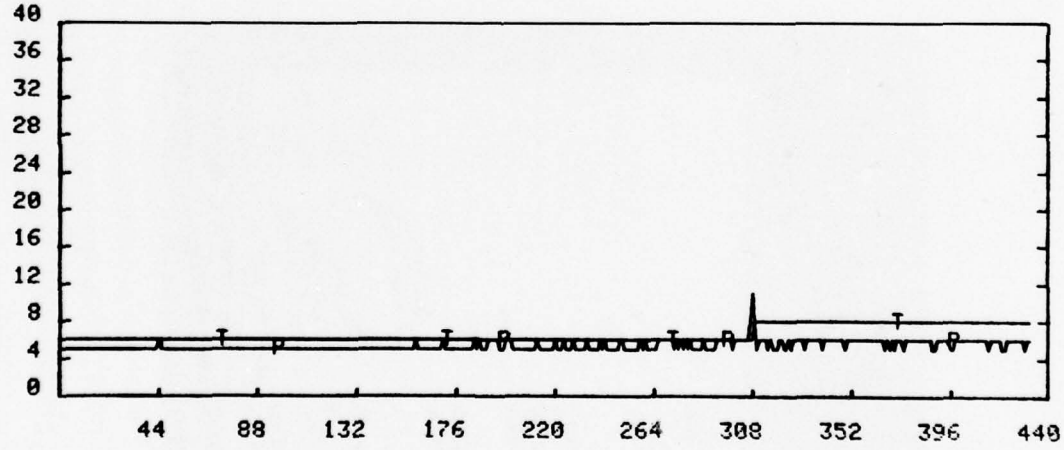


RESULT (b)

Figure C12. NOSC library acquisitions cover.



(a)



(b)

Figure C13. Acquisitions cover threshold profiles.

ILLUMINATION CORRECTION

Illumination correction is a digital compensation technique which provides a first-order restoration of nonuniformity of system response due to uneven illumination, $\cos^4$ losses, and sensor response variations. This is accomplished by storing digitized values of individual cell responses for an entire sensor line when a uniform high-reflectance target is presented to the imaging area and illuminated normally.

This technique, as executed in software in the Memory Control Unit (MCU) and in high-speed hardware form, is discussed in appendix C of reference C2 and in reference C3. The work was also presented as a paper to the SPIE Conference (ref C4).

VIDEO AMPLITUDE COMPANDING

Video amplitude companding is a process of redefining video amplitude level interval limits so that the total amplitude space can be described by a smaller set of numbers than needed to describe the originally partitioned amplitude space. In this manner the digitized video data are compressed, and may be transmitted with fewer digits than linear video. After the transmitted data have been received, the amplitude levels may be expanded to encompass the same range of levels of brightness originally encountered. In this manner the data are said to be companded.

There are sacrifices made in the quality of the reproduced images when the video is companded. If an amplitude zone is redefined to include a number of original linear brightness levels and given a single new designation to be transmitted, there is insufficient information to reconstruct the several original levels correctly at the receiving terminal. For example, if brightness levels 50 through 54 were redefined to a compressed (logarithmically) value of level 29, the receiver would have to be encoded to produce an output level, usually the highest of the range (54 in this case), upon receiving the digital signal level 29. There would be no information available to show that the true level should be 50 or 51. A consequence of this companding is a relative coarseness of the appearance of the image. As the number of grey levels is reduced, the boundaries between adjacent levels become more pronounced. This gives evidence of "contouring," since the boundaries represent levels of relatively equal brightness. The difference between 64 linear levels and a logarithmic companded image defined by 32 levels is detectable but not objectionable. When 16 log companded levels are used, the contouring becomes quite evident and somewhat objectionable. Images produced by using 8 levels or fewer have a definite artificial or synthetic appearance reminiscent of posters. This effect in the graphic arts and photographic industries is called "posterization."

The reduction from 6-bit linear data to 5-bit companded data offers a saving of only 17% of the buffer storage and channel bandwidth requirement if the data are transmitted uncompressed. Since the remaining partitioned brightness intervals each contain one or more of the original increments, even up to five in the higher brightness levels, companding may appreciably contribute to higher data compression ratios when run length or relative address coding techniques are used. Companding would not be used on black and white bilevel images, for which 1 bit per pel, properly thresholded, will suffice.

IMAGE DATA COMPRESSION

Experiments performed to date have only encompassed run length coding (RLC). Early results on compression were reported in appendix D of reference C2. The conclusions

C4. Real Time Correction of Acquisition Errors Applied To Solid State Scanners, a paper presented to the SPIE Meeting, August 1977, San Diego, California

drawn from this work indicate that converting the digitized pel amplitude data from binary to Gray code provided about a 30% improvement in compressibility. It was also shown that variable length RLC codes are superior to fixed length codes. Two problems were recognized during this test period. The first was that the imager produced a significant offset between odd and even pel amplitudes, thus shortening the lengths of runs, particularly in the less-significant bit planes. A second problem was an equipment limitation restricting run lengths to a maximum of 64 bits because of the number of accumulator bins in the Digital Image Analyzer (DIA). The compression ratios obtained during this period under these conditions were very close to 2:1.

Very recent data are reported in appendix D. These data were taken with a new and especially selected CCD121H imager having few blemishes and low dark current. The RLC data were compiled from a software routine rather than in the DIA so the 64-pel run length restriction was removed.

The new data included a repetition of the old straight run length data plus some novel investigations into a series of "meander" or "serpentine" experiments in which controlled excursions in the ±Y and −X axes were allowed while the run was continued generally across the X axis. The results of these experiments showed a significant improvement in RLC compression, especially compared to last year's results.

Relative Address Coding (RAC) is a new compression technique discussed in reference C5. For convenient access it is attached as an annex to reference C6. RAC exploits the redundancy of information from line to line. The sequence of transmission starts with the transmission of a line of data using RLC. The next line is composed by comparing the locations of changes from black to white or white to black in the new data line with the relative locations in the RLC line above. Because of the expected redundancy and similarity between lines, short codes are assigned to similar cross-overs and longer codes are used with the less frequent uncorrelated cross-overs. After a few lines of RAC (for example, seven) a line of RLC is transmitted. This line contains totally independent data and will correct for any errors accrued during the transmission of the previous seven lines. The authors of the paper show a table indicating a 2:1 improvement over RLC. The compression ratio is a function of scan density and is better at 8 pels per millimetre than at 4. NOSC is not presently experimenting with RAC but will be monitoring the progress of others utilizing it.

EDGE ENHANCEMENT

Edge enhancement has been shown to provide a rather dramatic improvement in the clarity and cosmetic appeal of typed copy. Two enhancement algorithms were tested. One was a recursive-type filter operating in two dimensions. The other was a nonrecursive filter also operating in two dimensions. The latter configuration was judged to provide more symmetry of enhancement and therefore to be the better candidate for hardware fabrication, since both filters require about the same quantity of hardware. A full discussion and example photograph are given in reference C2, appendix E.

The one-dimensional equation used to form the simple filter is as follows:

$$\frac{E_O}{E_I} = \frac{-K\ \ Z^2 + (1 + 2K\ )\, Z - K}{Z^2} \ ,$$

C5. Digital Fascimile Equipment, Quick-FAX Using a New Redundancy Reduction Technique, Yasuhiro Yamazaki, Yasushi Wakahara, and Hiroichi Teramura; R&D Laboratories of Kokusai Denshin Company, Ltd (KDD), Toyko, Japan, a paper presented at the National Telecommunications Conference (NTC 76), Dallas, Texas, 29 November–1 December, 1976

C6. Data Compression Report, NOSC Code 7323 Summary Report, September 1977

where K is a positive fractional constant which can be chosen to vary the amplitude of the enhancement effect.

This equation was used to formulate the two-dimensional equivalent which follows:

S_1	S_2	S_3
S_4	C	S_5
S_6	S_7	S_8

C = brightness amplitude of center pel

$S_1 - S_8$ = brightness amplitude of surrounding pels

Output, C_E = $C(2K + 1) - K$ (S highest + S lowest)

Unless $C \gtrless$ every member of the set S_n, in which case let $C_E = C$

The experiment showed that the enhancement was about optimum when the constant K was set at about 0.5. This provided a gain of 3.0 at the Nyquist limit. The low-frequency (dc) gain remains at 1.0 regardless of the gain constant value, K, chosen.

ACQUIRED IMAGE RECONFIGURATION

One of the important tasks in prestorage processing is the acquired image reconfiguration. A large number of imaging devices such as the Reticon CCPD-1728 and the RL-1872F, the Fairchild CCD121H and the CCD131, and the RCA TC1212 experimental time delay integration (TDI) device under contract by NOSC for the USPS all have multiple data output ports. Some are divided into odd/even sources. Others have four ports which simultaneously produce data from four adjacent or distinctly remote pel sites. Also, where two or more devices are used, pel data are usually received from both sensors simultaneously. This is the case with the Fairchild image acquisition equipment for the USPS in which two ports are available from each of two optically abutted CCD131 imagers simultaneously.

When such devices are used for the data acquisition, reconfiguration of the data is required at some point in the delivery of the data before arrival at the final document printer, unless of course the printer is designed to be ported exactly the same as the scanner(s).

There are a number of reasons for performing the reconfiguration as soon as possible after the data are acquired and digitized. Since most high-speed printers are designed to accept data in a raster line-at-a-time format, it is advantageous to convert the data to this format. All image processing algorithms of enhancement and data compression rely on relationships of adjacent pels for the high-speed execution of the processes. Therefore, it is most expeditious to have the adjacent pels stored in adjacent bytes and computer words where they can be conveniently and rapidly retrieved for algorithm execution. A final reason for desiring prestorage format in raster scan is that the data are then immediately available without processing or storage for presentation on raster-type displays.

Personality modules have been designed for several configurations of image data. These were discussed and described in reference C3. There are three configurations which will be required in the near future. The most useful at this time will be the personality circuit for the CCD121H imager which has odd and even pel ports. Another configuration will soon be needed for the Fairchild image acquisition equipment mentioned above. The third and most complicated personality circuit will be the formatter for the RCA TC1212 imager. This device can operate in either of two modes. The first is to provide four parallel outputs containing a group of pel data for four adjacent pels. The second is to provide four parallel outputs containing two groups of two adjacent pels. In this mode the first and second pel data are available from one port pair while the last and next-to-last pel data are available from the

other port pair. On the next clock cycle, the third and fourth plus the third-to-last and fourth-to-last pel data are available. The circuits designed for these imaging configurations allow data to be stored in an orderly manner in the frame-store memory (FSM) so that they can be withdrawn in raster format by simply sequencing (incrementing) the memory address register.

SCAN DENSITY INTERPOLATION

It is sometimes desirable to increase the apparent resolution of an acquired image. In a recent experiment, image tapes were being generated to demonstrate compatibility with an existing NOSC laser printing facility. The printer presently accepts 512 lines per inch resolution and can accommodate 4096 pels per 8-inch dry silver film width.

The CCD 121H presently mounted in the ICAS scans 1728 pels, usually at a resolution of 200 by 200 pels per inch in order to print copy of maximum possible width at as close as possible to a full-size original. Moving the lens and imager closer to the subject could produce 400 by 400 pels per inch if the Baldwin encoder output pulse rate were doubled. This would only have allowed the imager to cover one-half of the page with the 1728-pel scan width.

It was decided to leave the imager in the 200-by-200-pel-per-inch position. The Baldwin encoder output rate was doubled to provide the 400 pulses per inch in the direction of copy motion. It was also decided to interpolate between pels in the direction of line scan to provide a value of brightness for a synthetic pel halfway between each pair of acquired points. The value was determined by calculating half the sum of brightness of the two adjacent pels. Because of the increase in Baldwin encoder pulse rate, twice as many lines were read and stored on magnetic tape (4400 lines for an 11-inch original). Because of the acquisition-to-print resolution ratio (400:512), the image was only 78.1% the size of the original. The printed image showed no evidence that half the pels had been synthetically generated. No differences in horizontal and vertical resolution could be detected.

There were, of course, changes in the information content of the image as a result of both the interpolation in the direction of scan and the doubling of Baldwin encoder output in the direction of copy motion. The effect of interpolation between pels in a line of scan can be seen in figure C14. Without interpolation, the width of each pel is double that of the interpolated equivalent. Also, the video amplitude changes are abrupt when interpolation is not used. This causes the reproduced image to have the appearance of being constructed of blocks, unless the spatial frequency is close to the limits of visual resolution. It should be noted that interpolation adds nothing to the video bandwidth and that the Nyquist limit is not improved beyond that obtained in the original sampled data set. It should also be noted that interpolation should not generally be classed as a prestorage process for USPS systems. Interpolation before buffer storage and transmission increases the capacity requirements of both. Therefore, the data should be interpolated after transmission with real-time hardware just before storage in the final print buffer.

The increase in sampling frequency in the direction of copy motion does provide an increase in the resolution of the acquired image. Scanners such as the RCA TC1212 and the Fairchild CCD121H are constructed with square photosites. The CCD121H photosites, for example, are 13-μm (0.52 mil) squares located on 13-μm centers. When the optical ratio of 5 mils to 0.52 mil is set to provide the 200-pels-per-inch resolution at the document, the portion of the document included in the square imager photosite in the direction of copy motion is also 5 mils (at any single instant in time). If the imager is exposed to the copy during the total time between two Baldwin encoder outputs representing incremental motion of

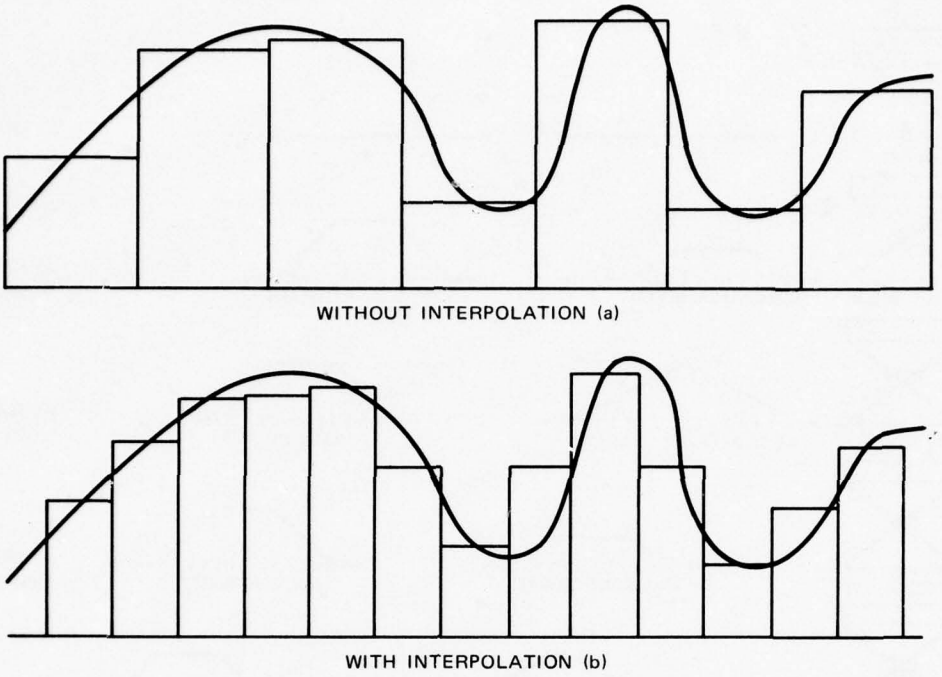


Figure C14. Effect of linear interpolation on a video waveform.

5 mils, then the imager is collecting light over a 10-mil copy space in the direction of copy motion. The actual time duration that each small spot within the 10-mil space provides an illumination contribution to the imager is dependent on its spatial relationship to the encoder pulse locations. Figure C15 shows the effect of copy motion on imager response. The column of five diagrams of the imager, lens, and copy on the left side of the figure depicts the portions of the copy which are imaged onto the scanner at the start of a sequence of acquisition and at four consecutive spatial intervals of 0.0025 inch thereafter. For simplicity, a hypothetical imager having 5-mil-by-5-mil photosites and a 1:1 focal distance has been substituted in the diagram for the 0.52-mil-by-0.52-mil photo area of the real Fairchild imager which would use a 9.615:1 optical reduction in the lens system.

The center vertical sequence of waveforms depicts the development of imager response relative to specific points on the copy. For example, after 0.0025 inch, the point "E" on the copy has moved from focusing on the center of the imager to a point on the extreme right edge, and will not be in the field of view after this time. Consequently, the amplitude of the waveform in the center column will never increase after this time. Point "I", however, which started at the very beginning edge of the field of view, focuses on the exact center of the imager after a motion of 0.0025 inch. Illumination will be seen from this point during the next copy motion interval of 0.0025 inch. Consequently, the contribution of point "I" to the total response of the imager is higher than that of all other points and forms the apex of the triangle in the second interval of the center column of figure C15. If the imager is read out after a motion of 0.005 inch, the contents of the imager are then reset to zero, and the process begins to repeat, this time on a new area of copy. The relationship of three sample space intervals and three readouts is shown as the bottom center set of curves. This analysis shows that 25% of the imager response actually was contributed by copy areas outside the

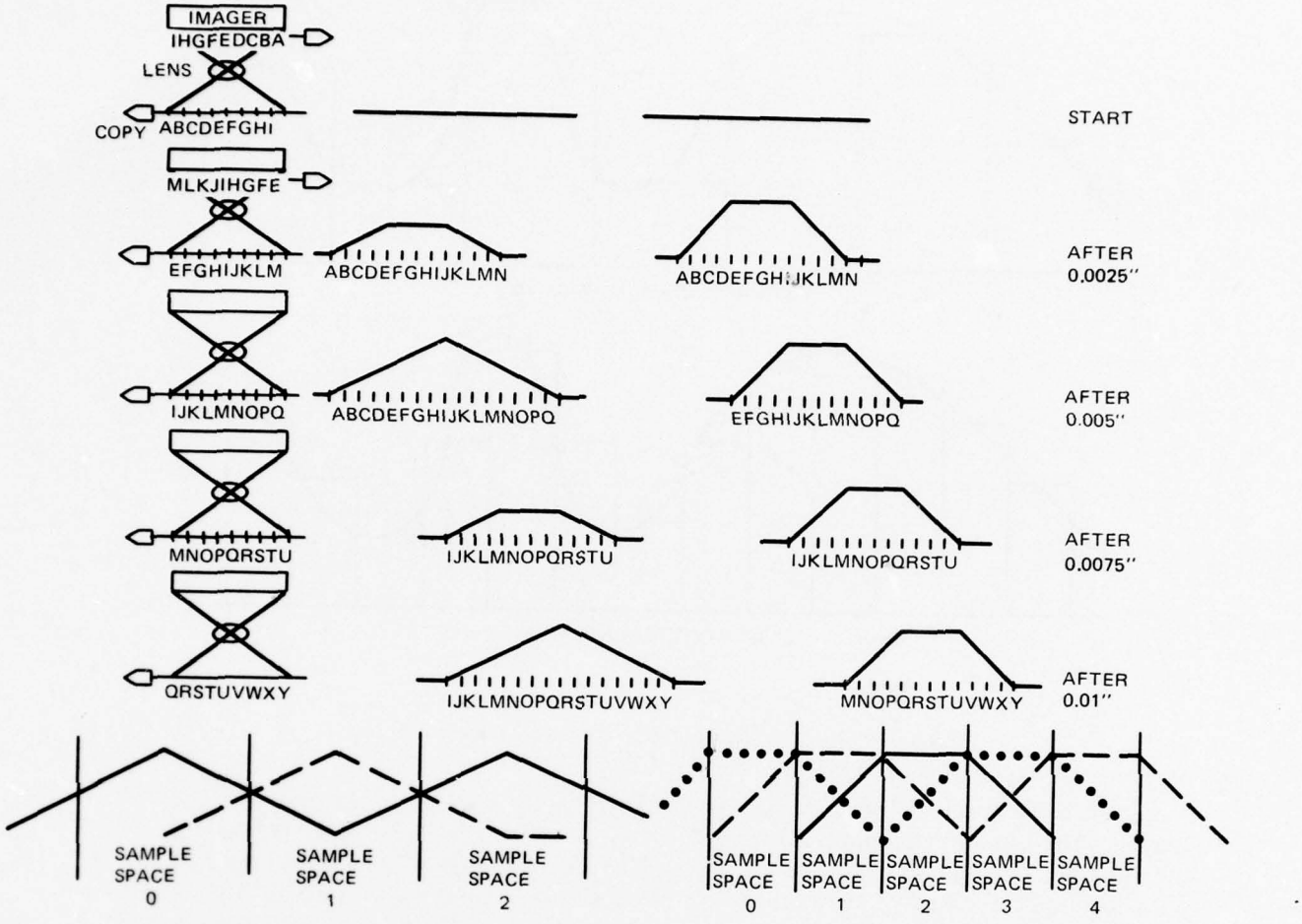


TABLE OF CONTRAST TRANSFER FUNCTIONS

Scan Frequency lines/inch		Copy Spatial Frequency, lines/inch				
		66.7	100	133.3	200	400
200	Best	1.0 CTF	1.0	0.75	0.5	0.0
	Worst	1.0	0.75	0.65625	0.0	0.0
400	Best	1.0	1.0	1.0	0.75	0.0
	Worst	1.0	1.0	0.875	0.5	0.0

Figure C15. Comparison of imaging performance—200 vs 400 lines/inch.

intended sample space. This then limits the contrast transfer function (CTF) best case to 0.50 at the Nyquist limit. The worst case with the black and white copy interval boundaries falling at the apexes of the triangular intervals is zero. At exactly this phase the imager output would be constant at a level representing the grey average between the white and black levels of the 200-pel-per-inch Nyquist test copy. If test copy containing spatial frequencies of higher resolution than 200 pels per inch is run, any imager response is simply due to aliasing.

A second set of waveforms is shown on the right side of figure C15. The purpose of these is to show the consequences of sampling at spatial increments of 0.0025 inch rather than 0.005. At a given document velocity the time required to transit 0.0025 inch is half that of the longer sample interval. With half the integration time, the system sensitivity must be doubled, through either doubling the range of copy reflection density or increasing the postdetection amplifier gain. Doubling the gain allows the area under the first right-hand waveform to be twice that of its counterpart in the middle column. Since the accumulated charge is dumped each 0.0025 inch, this is the residual spatial response for that interval, and the relationship of several intervals and their overlaps is shown at the bottom of the figure for comparison to the triangular waveform set obtained from scanning for 0.005 inch.

The resolution of the right-hand set of waveforms is appreciably better than that of the center set. A number of spatial frequencies were used to calculate the relative performance of the two sampling intervals. The results of the comparison are shown in the table at the bottom of figure C15. Increases in CTF for the examples sampled at 400 pels per inch are evident for the higher spatial frequencies.

The consequences of sampling at the higher spatial scan density should be considered carefully. The advantages are obvious. Smearing of the image due to copy motion is reduced and the resolution is then approximately equal to the resolution in the direction of scan (normal to copy motion) at about 100 lines per inch. The disadvantages, as mentioned previously, are the increases in required storage capacity and transmission bandwidth. A similar improvement in smear reduction could also be made by employing an imager having a rectangular pel area. Narrowing the aperture dimension in the direction of copy motion improves the CTF at the expense of loss of scanner sensitivity.

The need for resolution improvement should be examined carefully before any commitment to hardware is considered. Any expensive or complicated processing to gain spatial frequency response beyond the resolution of the viewer's visual acuity at normal viewing distance or beyond the legibility of the copy printer would be an unwarranted extravagance.

SYSTEMS INTEGRATION TRADEOFFS

Since the concept definition study for EMSS is not yet completed, the specifications for the imaging requirements cannot be fully stated. Some of the requirements are reasonably certain and can be used to establish some baseline criteria. Requirements falling in this category are:

1. The paper size will be 8 1/2 by 11 inches.
2. The imaging speed will be 10–20 pages per second.
3. The (or one of the) imaging resolution(s) will be about 200 by 200 pels per inch.
4. The basic system will accommodate at least two-level (black and white) images.

MINIMUM FUNCTIONAL SYSTEM

Based on these requirements, a system somewhat like the scanner subsystem under development at Fairchild, Syosset, may suffice. Because of the paper-handling restriction, this system scans the paper along the 11-inch dimension. It presently employs optical abutment of two 1024-bit CCD131 imagers to provide a scan width of 10.24 inches at 200 pels per inch. The illumination system utilizes two slit aperture fluorescent lamps. Analog adaptive thresholding is used to produce bilevel (0 and 1) output states for the white and black states of the copy materials without a requirement for illumination correction. The imager subsystem is being designed to operate at up to 10 pages per second. A three-page solid-state buffer memory is used to reconfigure the image data into a raster format for transmission and printing. The pel rate (and in this case the bit rate) is 41.8 megapels (megabits) per second. The system is expected to accommodate typed pages, legibly handwritten messages either in pencil or ballpoint pen, black and white line drawings, or any other document which will provide a print contrast ratio (PCR) of 0.3 with a detector system having approximately uniform sensor response over the visible spectrum. Print contrast ratio is defined as

$$PCR = (r_{max} - r_{min})/r_{max}$$

where r = reflectance from the copy.

GREY SCALE SYSTEM

A system such as that described above offers an excellent performance-to-cost ratio where the input is known to be black and white readable copy having a reasonably good PCR. If the requirement is added that black and white continuous-tone (photographic) or multiple-grey-scale images must be acquired, the equipment quantity and complexity increase appreciably. The illumination standards must be greatly improved, or, alternatively, the optical-to-electrical conversion subsystem must be corrected by prestorage processing.

With a good adaptive threshold algorithm, bilevel images quantized to only 1 bit per pel can be satisfactorily acquired in the presence of 30-50% droop in illumination profile, "cosine fourth" law degradation, and individual scanner pel sensitivity differences. However, these ranges of response variations cannot be ignored if continuous-tone images or black/grey/white images are to be acquired with eight or more grey scale levels. Since most continuous-tone images are acquired at 64 or more grey shades to prevent contouring, variations of illumination levels or imager response of 2% or more will affect the quantized values of the digitized image. "Cosine fourth" effects with the 55-mm Nikon lens in the test bed result in a 6.6% fall-off at the 10.5° edge angle of the copy. The illumination also falls off at the edges because of the finite length of the special fluorescent tubes and the lamp enclosure. An optimum solution to overcome these two variations is to design a compensating illumination

system which not only provides even illumination, but also increases the light level at the edges to equalize the cosine fourth losses. Such approaches as variable-width shutters and variable neutral-density filters are candidates. At present, the stability of such an illumination source is not predictable because variation of illumination output from one fluorescent lamp to another is not known, nor are there sufficient data regarding the decline in illumination output as a function of position along the tube or time in service at various drive levels. It is felt that the best performance will be obtained from the system if an optical illumination compensation system is employed to provide at least a first-order balance of response from the imager. The reasons for this are somewhat subtle, and the consequences were not fully evident until the latest compressibility study was in progress.

The ICAS has been providing illumination correction for over a year, using a software algorithm in the MCU processor. A design is complete for a real-time hardware equivalent equipment to perform the same function in real time.

During the compressibility study, the same run length compression algorithm was run on a captured image both before and after illumination correction. The uncorrected image had somewhat greater compressibility than the corrected version. At first it was felt that this unexpected result could be attributed to nonuniformity of the white standard target. For this reason several attempts were made to reduce artifacts from the white standard profile. The spatial line sample interval for acquiring the white standard averages was increased so that small blemishes would not be sampled more than once. The lens was defocused for some tests so that the point spread function area was increased. A software curve smoothing algorithm was applied to the illumination profile for other experiments. The uncorrected image always had slightly higher compressibility than the corrected version. In most cases, it was the least-significant bit plane which contributed mostly to the increase. It is now suspected (but not a conclusive fact) that the expansion of the drooping edge pel amplitudes also amplifies the first difference statistics in these regions, thereby decreasing the lengths of runs, particularly in the low-order bit planes. Therefore, if this is the case, coarsely correcting the illumination levels to produce an approximately constant electrical output when scanning the white standard target will improve the system performance and the effectiveness of the illumination correction algorithm, if it is required. It is possible that optical illumination correction alone may provide images which are undetectably different from those having the full digital illumination correction, both to the viewing subject and in analysis of the compressibility. In this case, the digital compensation scheme should be preempted by optical correction. This test will be included in the future work for FY78. In any case, a system acquiring grey scale images with adequate quality will require some form of illumination compensation, optical and/or digital.

An optical subsystem which is a candidate for the grey scale systems is the edge enhancement hardware. The current nonrecursive enhancement algorithm described earlier in this report acts to modify a pel brightness level by either increasing or decreasing its value as a function of the amplitudes of its eight surrounding neighbors. Pels having a brightness level exactly halfway between the brightest and dimmest of the eight surrounds are not changed. Those having values slightly lower than this midpoint are further reduced and those having values above the midpoint are increased. The amount of decrease or increase can be modified by changing the gain constant of the algorithm. Given a black and white image with perfectly even illumination and a perfectly selected threshold to acquire a bilevel image, edge enhancement will add nothing to improve the selection of pels which fall into the upper or lower segments of the two threshold levels. However, in most cases the illumination will not be perfectly flat – the copy has small variations in reflection density, and the threshold algorithm will seldom be chosen to fall exactly on the midpoint of the black and white range. If any or

all of the above are true, then edge enhancement will improve even the simple bilevel acquisition process. The gain in legibility and cosmetic acceptance of black and white copy acquired with multiple grey scale levels has been demonstrated and is reported in reference C2.

Reference C2 also presents a discussion and the results of video companding in appendix E. This study showed that a 4-bit companded image had objectionable contouring but a 5-bit companded version could produce a quite acceptable grey scale image. The use of 5 bits per pel versus 6 offers a 17% reduction in frame-store memory (FSM) capacity and transmission channel bandwidth. As discussed earlier in this report, it is felt that there will also be a large improvement in the run length compressibility of the compressed image. This premise will be tested when time permits in FY78.

No mention has been made regarding the basic requirement for FSM in either of the foregoing system descriptions. Capacity requirements for bilevel and 64-level image storage are 3.74 and 22.44 megabits per page, respectively. Such memories are expensive. They are also the principal contributors to restrictions in mean time between failures (MTBF) of a USPS operational imaging system. The digital bit stream rate for 20 grey scale pages per second is approximately 500 megabits per second. This rate approaches a saturation rate for even the most sophisticated dedicated satellite communications system. The least expensive and most reliable way to store a document image is to retain the original copy itself. The only drawback to such a system is that this requires a high-speed demand feed paper-handling system in order to prevent an appreciable overhead time at the start of each postal center's allotted transmission interval on the time division multiple access (TDMA) satellite link. If each center's time slot is of fixed lengths, then a predicted lead time could be added to the paper feed timing cycle to have copy ready when the slot is available.

There are, of course, other advantages to FSM at the transmitting site. First, having a full-page memory allows only valid full-page images to be committed to the transmission and ultimately to the printing equipment. Second, the transmitting speed can be isolated from the acquisition speed. The 1-inch gaps between the 11-inch pages are essentially dead time to the transmission and output systems. Therefore, the output rate can be reduced by 8.3% by using FSM. The inertia-free capability of semiconductor memory allows the output message to begin exactly on external demand and to continue on electronically controllable interval or remote clock synchronization. The tradeoffs for the needs of FSM cannot be resolved until several of the EMSS concept decisions such as demand paper feed, link cycle protocol, receiving center FSM, and printing methodology are frozen. If doubt exists about any of the above, FSMs are a requirement for both of the above systems and the system which will be described next.

FULL-COLOR SYSTEM

A very high-performance image acquisition and processing system must be used if full-color acquisitions are to be included in the EMS system. Figure C16 is taken from appendix A of reference C2. This figure is intended to depict a system offering the most stringent controls on quality of acquired images and optimum analysis during a prescanning examination of the copy. The analysis results would be used to control illumination, enhancement techniques, scan density, gain and level, and compression algorithms to be used during the main scan acquisition of the copy.

A detailed explanation of the operation of the system is included in appendix A of reference C2. Only a few paragraphs outlining the acquisition strategy will be included here for continuity.

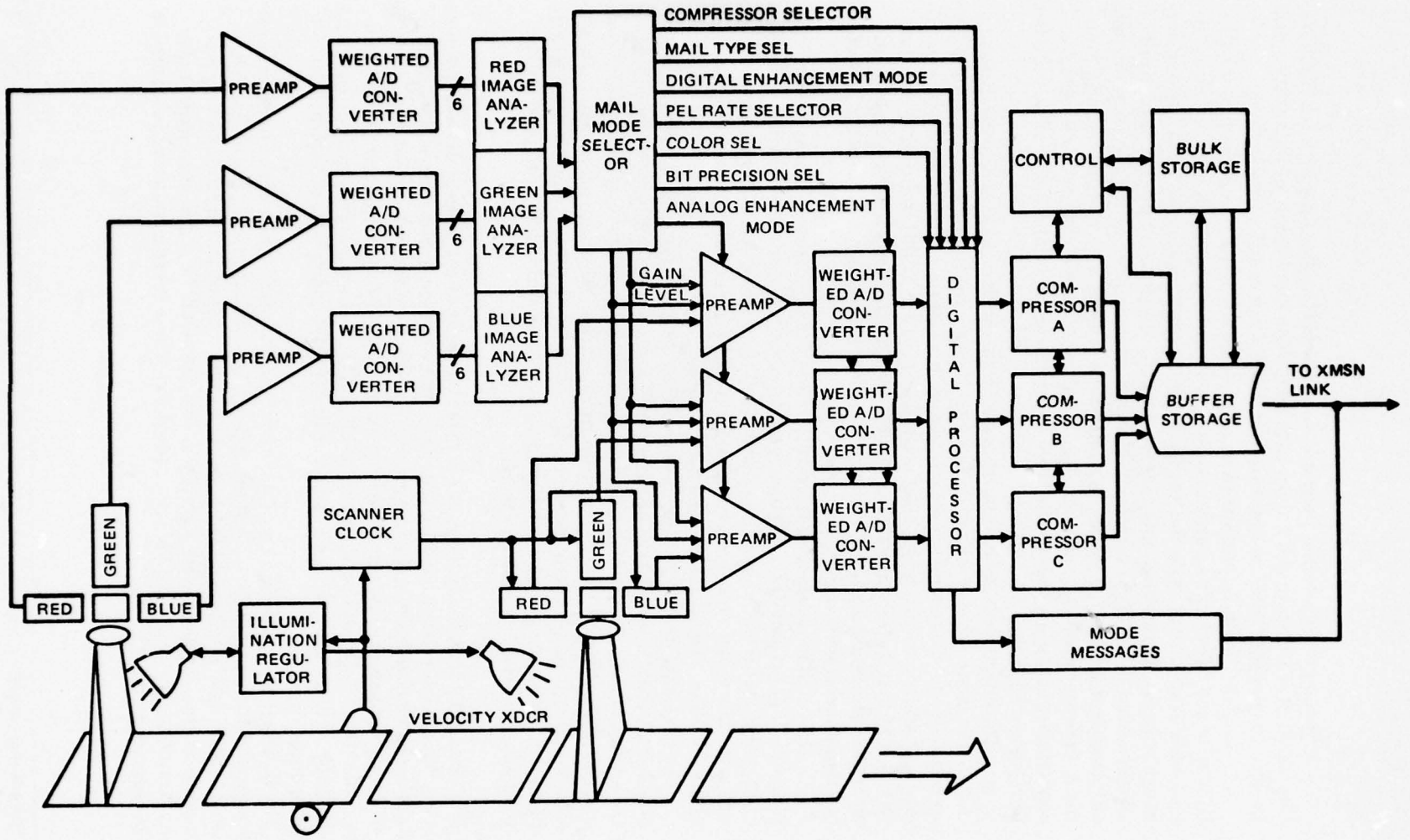


Figure C16. Advanced electronic message input terminal.

At the prescan station there are three image sensors – one with red illumination, another with green, and a third with blue. The three colors of illumination will be used for possible contrast improvement and for future color applications.

Each of the three outputs from these sensors is fed into a preamplifier with fixed gain and offset. The gain and offset on all three preamplifiers are adjusted so that when black velvet, with the lowest possible reflectance, is placed in front of the image sensors, the resulting output from the preamplifiers will produce an output of all zeros from the A/D converters; and when a white surface of $BaSO_4$, with the highest possible reflectance, is placed in front of the sensors, the resulting outputs from the A/D converters will be all ones. The weighted, or nonlinear, A/D converters will convert data according to Weber's* rule to minimize the total number of bits needed to represent each pel.

The image analyzer is a statistics gathering machine used to supply image data to the mail mode selector where various decisions are made to properly set up system controls for the main scanner stations. At the present time a requirement is seen to generate statistics which include pel brightness statistics (PBS), run length statistics (RLS), and first difference statistics (FDS). Preliminary tests may generate requirements for additional statistics which may include time-dependent statistics and various two-dimensional codes.

The mail mode selector is a decision unit for the main scanner system control. It accepts inputs from the image analyzer and uses them for the following: gain and offset adjustments of the main scanner preamplifiers; selection of enhancement modes, which may be either digital or analog; selection of type of data compression; selection of bit precision; and selection of image resolution. . . .

The image analyzer in the advanced electronic message input terminal as proposed must analyze data from the three image sensors at the prescan station simultaneously. It must accumulate all types of statistics simultaneously. The NELC image analyzer to be discussed is designed for one input channel and to accumulate the different types of statistics, one at a time. It is designed to accept data at a channel rate of 21 megapels per second. Four or more channels will be required to produce the total 84 megapel per second design goal.

It is envisioned that the outputs of the three channels of the main scan station will be available for three types of transmission. The first choice will be to enhance, compress, and store all three channels separately for transmission of full-color data. A second choice will be to mix all three channels into a single image representing panchromatic system response for the copy. The third choice will be to select the channel for which the PBS analysis shows the highest contrast. This image may then be sent with the 64 levels (6 bits) or thresholded into a single-bit-per-pel format.

The ICAS system at NOSC does not contain the necessary hardware to provide a real-time emulation of the entire system shown in figure C16 simultaneously. Each function shown in the figure can be accomplished in software, and most of the functions have been tested to some degree. A much more rigorous investigation will be required to select those functions needed for the definitive EMS specifications. These investigations are scheduled in the FY78 statement of work.

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*Not Weber's fraction, but a geometrically proportional step increase for successive grey levels.

RESULTS AND CONCLUSIONS

1. A number of prestorage processing techniques have been studied with promising results. These include:

   a. Prescan analysis
   b. Automatic gain and level control
   c. Adaptive thresholding
   d. Illumination correction
   e. Video amplitude companding
   f. Image data compression
   g. Edge enhancement
   h. Acquired image data reconfiguration
   i. Scan density interpolation

2. The applicability of these processes to three systems having different levels of performance has been discussed.

3. A number of these processes have interactive effects and should be tried in groups of two or more. One example is video compression followed by one or more of the serpentine compression algorithms. Another example is hardware improvement in uniformity of imager response by modifying illumination source followed by the final software or hardware illumination corrections.

FUTURE NOSC PLANS

1. Expand the data base on performance of image analysis and prestorage processing techniques.
2. Study the benefits of temporal analysis of data for determining document classification (bilevel vs continuous tone).
3. Study the benefits derived from flattening the imager response by adding auxiliary illumination sources to page edges.
4. Produce bilevel and continuous-tone images using log compressed 5-bit video. Compare the compressibility with previously analyzed linear video images.
5. Apply the NOSC edge enhancement algorithm (which is a high-frequency two-dimensional spatial filter) to continuous-tone images and observe effects on clarity and interpretability.
6. Continue to refine existing prestorage processing techniques and study others which offer improvement in quality, throughput, or cost for postal applications.

APPENDIX D: DATA COMPRESSION

Prepared for

US POSTAL SERVICE

October 1977

NAVAL OCEAN SYSTEMS CENTER

San Diego, CA

CONTENTS

INTRODUCTION

Data compression technology investigations on previous agreements have been principally related to simple run length coding (RLC) methods of compression. A summary data compression report covering this work was submitted during the past year and is included in appendix D of last year's annual report.*

An attempt was made to provide consistency to the method of obtaining the data so that data taken during these experiments could be related back to the previous results. In retrospect it is now clear that very little of last year's work can be correlated with the present results. One of the same documents, the typed page, was used in both years' experiments, scanned at the same resolution, and analyzed for both binary and Gray encoding as before.

Here the similarities end. It has been determined that the compressibility of grey-scale images using RLC techniques on each of the bit planes is very, very dependent on system noise. In the interval between the data acquired for last year's results and the data used for these tests, many changes have been made in the system. A new imager, the Fairchild CCD 121H, has been substituted for the older CCD 121. This greatly reduced (but did not eliminate) a problem of difference of response of odd- and even-numbered photosites from the imager itself. The fact that the new device contains an on-chip amplifier having about seven times the gain of the older device caused the video amplifier electronics to be changed.

Failure of the older analog-to-digital (A/D) converter and the timely arrival of the new high-performance units further changed the distribution of data into the bit planes.

Modifications were made to the procedures for illumination correction which greatly reduced the problem of the introduction of artifacts into the illumination profile by non-uniform reflectance from the white standard calibration target. This same modification (smoothing) helped improve the compressibility to some extent but absolutely precluded elimination of the last traces of differing response of the odd-numbered/even-numbered photosites.

A decision was also made to remove the restriction of maximum run lengths of 64 pels, which was a constraint required by the hardware digital image analyzer (DIA). Since very long runs were expected using the "meander" technique, which will be discussed in detail in this report, it was decided to acquire the run length statistics (RLS) through the Memory Control Unit (MCU) by using a software program.

Although the results obtained were only equal to those obtained elsewhere in image compression studies, there is enthusiasm to continue the experiments after characterizing the entire acquisition path from white standard, illumination source, imager, video preamplifier, buffer line drivers, and gain and level circuits and through the A/D converter. Once this path is as noise-free as it can be made and the remainder of its characteristics are well understood, more promising results are expected. Combinations of video log compression, followed by combinations of meander compression patterns, should result in significantly better compression ratios. The following year's work agreement allots adequate time for participation in this task.

TESTS PERFORMED

ILLUMINATION CORRECTION

Tests have been performed to examine the bit precision requirements for the calibration values stored in a look-up table used for software simulation of the illumination correction

*Second Annual Report, Advanced Mail Systems Scanner Technology, NELC Technical Report TR 2020, October 1976.

algorithm. Prior to the generation of data for this report all evaluations were subjective, indicating very little difference in image quality at bit precision above 7 bits, the range tested being 6 to 10.

As will be shown in a later section, the illumination correction procedure as implemented previously was found to introduce additional artifacts into the corrected image data which decreased the compressibility of the image. The measure by which this determination was made is the compression ratio calculation performed on the run length statistics from uncorrected and corrected images.

In order to investigate the decrease in compressibility after illumination correction, several different illumination curves—calibration values—were generated and used to correct the Typed Page image. In an attempt to avoid any possible artifacts from the white standard, a calibration curve was generated from the white standard with the lens defocused. Figures D1 and D2 show examples of a calibration curve with the lens focused and with the lens defocused, respectively. Each of these curves was obtained by scanning the white standard and summing 16 individual lines, each spaced about 25 lines apart. This procedure is used in an attempt to average out any artifacts or imperfections in the white standard. As can be seen in the two figures, there is a small difference in the two curves but not a significant one. When used for illumination correction, the calibration curve produced from the defocused lens made a slight improvement in the compressibility of the image.

A second test was made by smoothing the original calibration curve. Figures D3 and D4 show the results of smoothing with a 3-pel average and an 11-pel average, respectively. Using these calibration curves made a more significant improvement in the compression ratio calculations for the image tested. Thus, calibration curves similar to figure D4, with 11-pel averaging, were used for the illumination correction of the images used for analysis in this report. A new calibration curve is generated each time an image is scanned.

RUN LENGTH STATISTICS

Since, at the writing of this report, the Digital Image Analyzer (DIA) was undergoing modification, the Memory Control Unit (MCU) was used to generate the run length statistics. Also, since these statistics are generated by software in the MCU, the hardware limitations in the DIA (see NELC TR 2020, Second Annual Report) may be circumvented, allowing runs of all possible lengths to be analyzed in the test images. This will allow much more accurate calculations to be made of the compression ratios by using the variable-length run length codes.

Now that statistics can be generated on run lengths of up to 1700, or longer for the meander statistics described in the next section, a new method of presenting this volume of information is presented here. Figure D5 is a group of six log-log plots, one for each bit plane, showing the run length statistics for a typical image. In these plots, a single point is plotted for each nonzero entry in the table of statistics. The three cursor marks (arrows) in each plot divide the total number of bits, 3.74 million for an 8½-by-11 inch page, into quarters for each bit plane. The position of these cursor marks, measured along the vertical axis on the plot gives an indication of the potential compressibility of the particular bit plane. The higher the cursor marks on the plot, the greater the resulting compression. The general characteristic can easily be seen that the lower bit planes contain many very short runs and the higher bit planes contain many long runs.

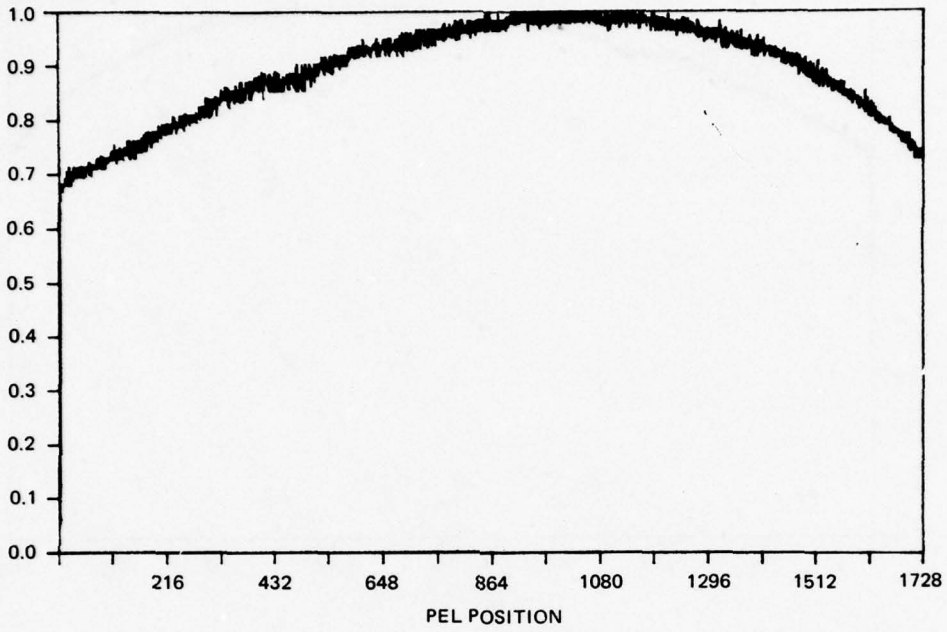

Figure D1. Illumination profile, 09/12/77, 10-bit, focused, NOSC #34, file 0.

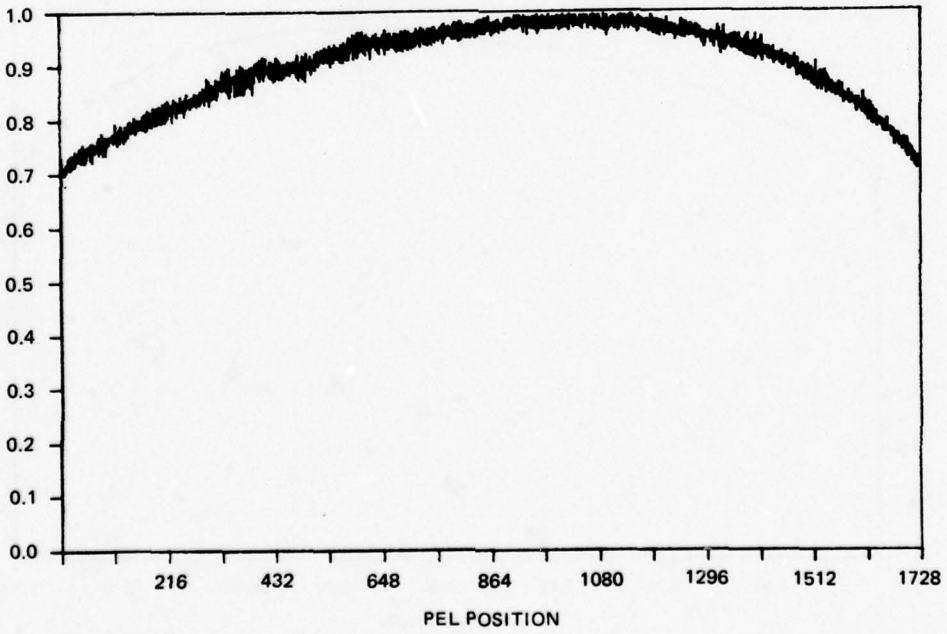

Figure D2. Illumination profile, 10/03/77, 10-bit, defocused, NOSC #35, file 3.

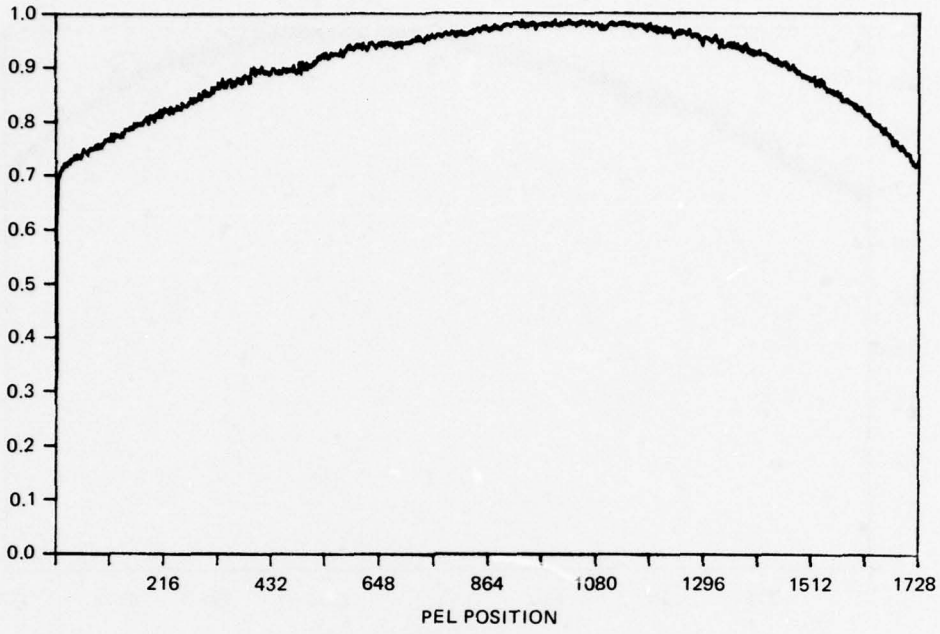

Figure D3. Smoothed illumination profile, 10-bit, 3 pels averaged, 09/15/77.

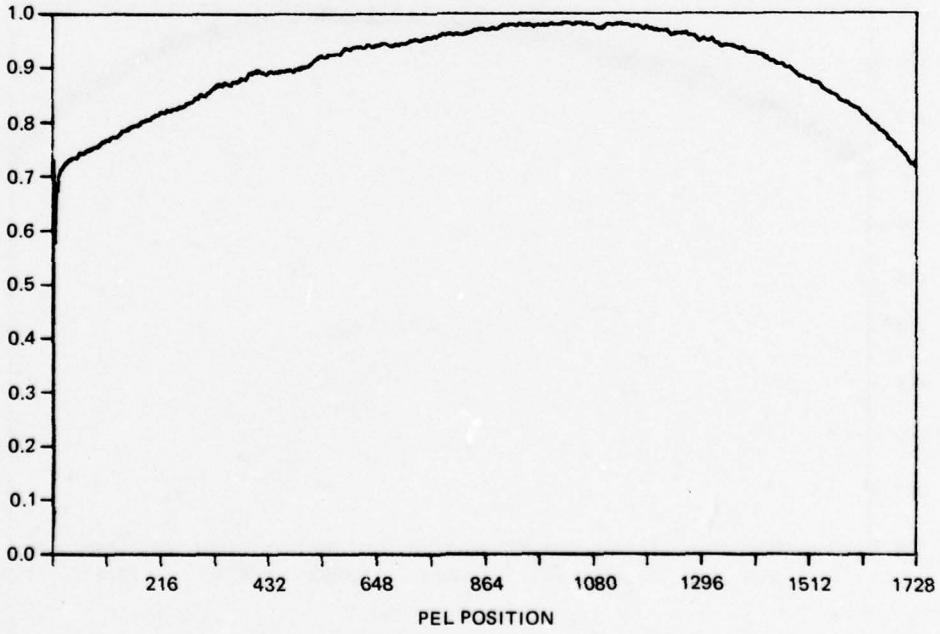

Figure D4. Smoothed illumination profile, 10-bit, 11 pels averaged, 09/27/77, NOSC tape #35, file 01.

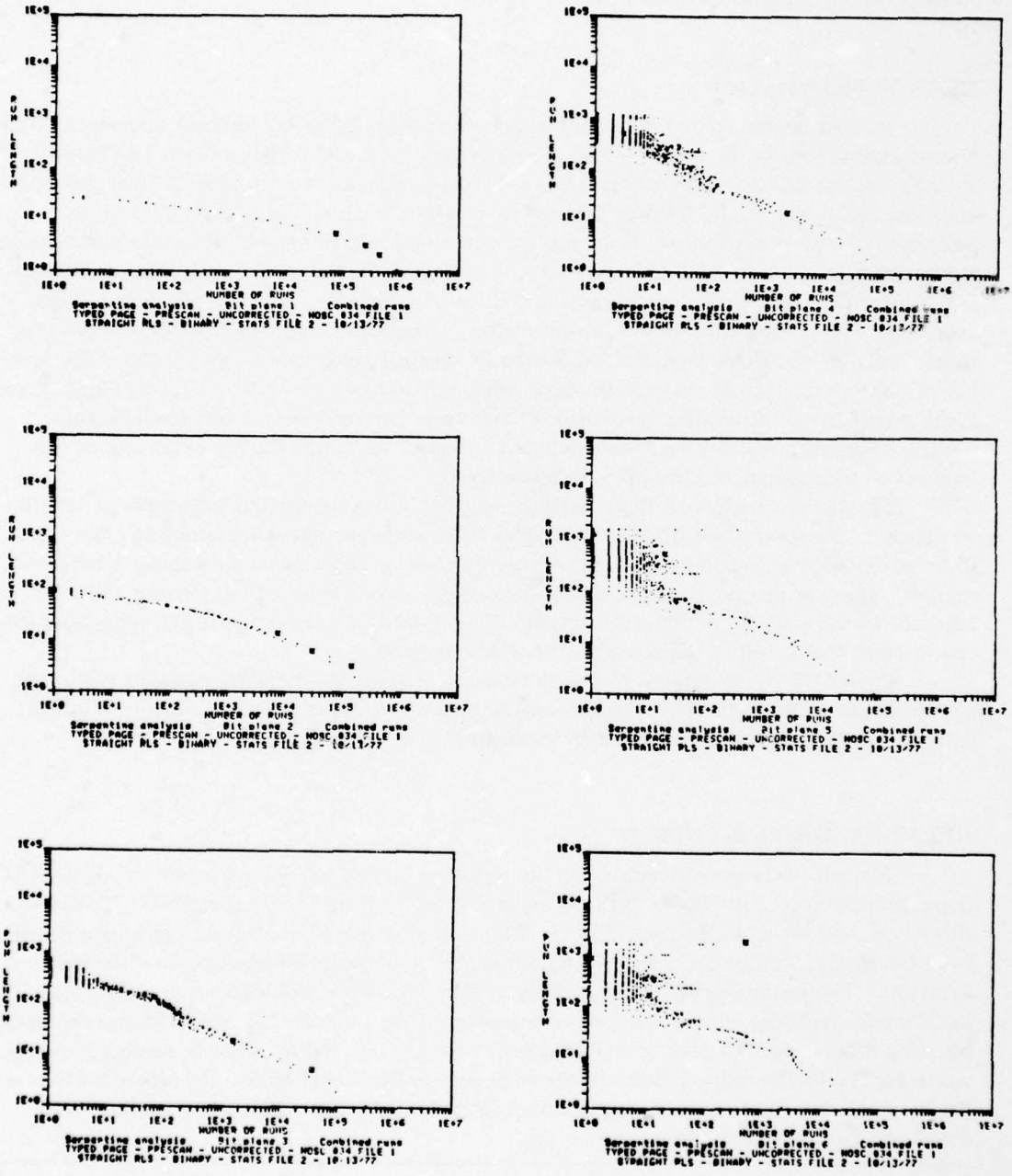

Figure D5. Run length statistics.

It should be pointed out that what appear to be vertical lines in some of the log-log plots, or scatter diagrams, are actually individual points spaced closely together so as to appear to be continuous lines. Also, the spacing of these groups of points in the first horizontal log cycle is due to the fact that there can only be integral numbers of runs; eg, there cannot be 2.5 runs of a particular length. In order to further understand how these log-log plots were generated, annex A has been included, which contains a numerical listing of all the data for each of these six bit planes. Each entry in this listing will correspond to a single point in the log-log plots on figure D5.

MEANDER STATISTICS

In most images there tends to be a high correlation between adjacent lines; ie, a given line will have close to the same brightness characteristics across it that its near neighbors have. It therefore should be possible to combine two or possibly more lines and perform run length encoding on them in some fashion, taking into account the high correlation in the near neighbors of a picture element. Several different patterns have been investigated to determine any possible increase in the compressibility of an image. These are shown in figures D6 and D7. Figure D6a shows the normal pattern followed on a single line when doing run length encoding. Figure D6b shows the simplest of the "serpentine" patterns taking two lines at a time. It can be visualized that in a white area on a typed page, runs of length twice the number of pels per line can be generated. Also, when encoding characters on a typed page, there is the possibility of generating black runs of twice the length as before due to the highly vertical nature of most typewritten characters. Figures D6c and D6d are extension of this concept to four and eight lines of data, respectively.

To obtain statistics on these patterns, a program was generated to gather run length statistics on images in these and other formats. The program allows from one to eight lines to be analyzed at a time and a pattern may contain up to 16 straight line segments before it repeats. There is also the restriction that the end pel of one cycle of the pattern must be adjacent to the start pel of the next. Figure D7, referred to as a double spiral, represents a worst-case pattern that can be analyzed with the ICAS program.

Figure D8 was generated to demonstrate the size of the meander patterns relative to a typical typewriter font. The numbers beside the two meander patterns indicate how the pattern is entered into the processor at the beginning of an analysis.

RELATIVE ADDRESS CODING

No tests were performed during the reporting period on relative address coding (RAC), but a paper presented recently at the National Telecommunications Conference (NTC 76) discusses this novel method of data compression.* Rather than attempt to abstract significant details as to the methods and results to date, a copy of the paper is included as annex B to this appendix. The promising results, especially at 8 by 8 pels per millimetre (approximately 200 by 200 pels per inch), where ratios of compression of better than 2:1 over RLC are obtained by using relative address coding, would offer an appreciable reduction in transmission bandwidth for the forthcoming Electronic Message Service System (EMSS). Results of further studies made by others actively engaged in testing the RAC algorithm will be followed in detail and discussed in future reports.

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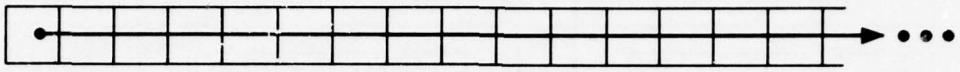
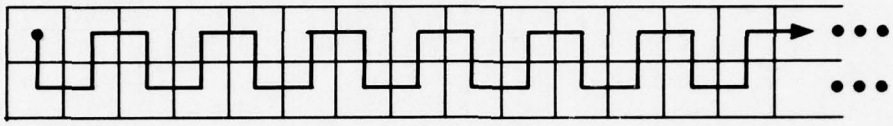
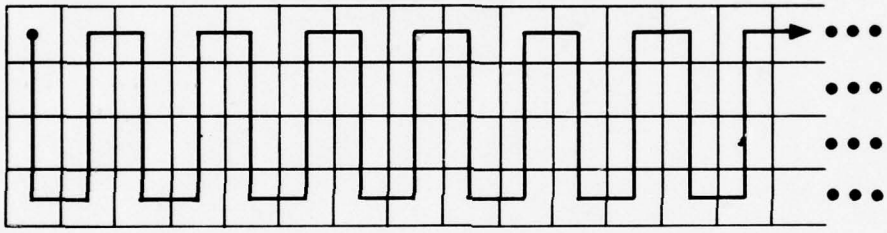
*Digital Facsimile Equipment "Quick-FAX" Using a New Redundancy Reduction Technique, Y Yamazaki, Y Wakahara, H Teramura, R&D Laboratories, Kokusai Denshin Deniva Co, Ltd (KKD)



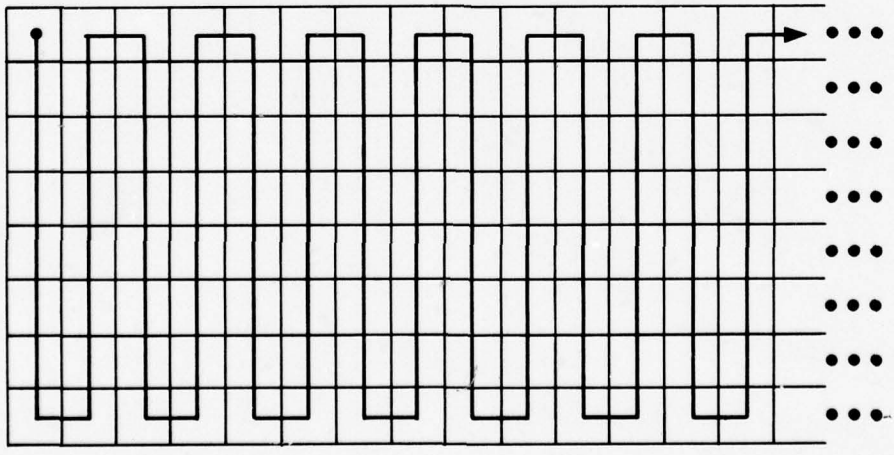
a. STRAIGHT RUN LENGTH



b. TWO-LINE SERPENTINE



c. FOUR-LINE SERPENTINE



d. EIGHT-LINE SERPENTINE

Figure D6. Meander patterns.

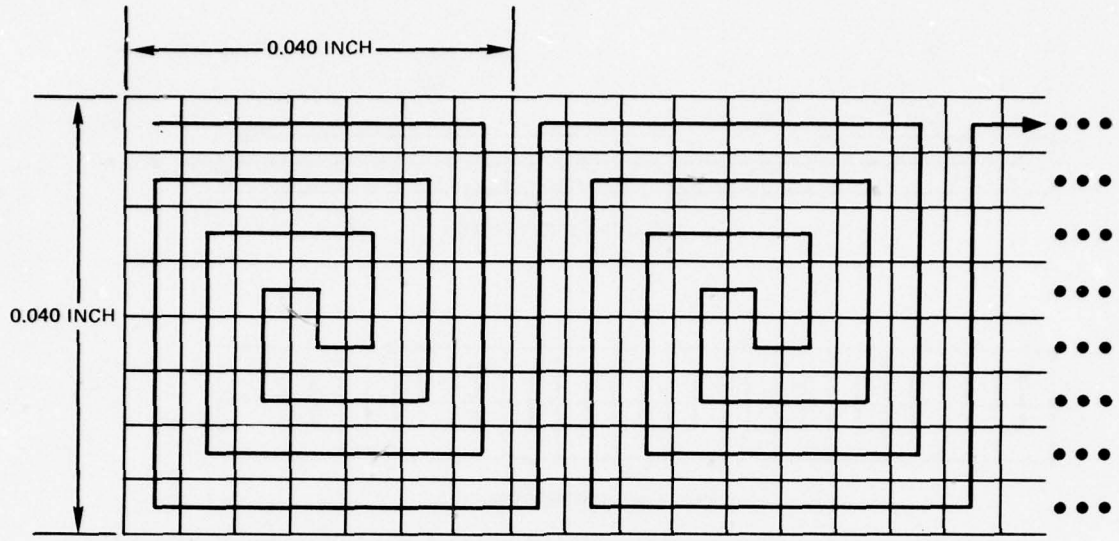
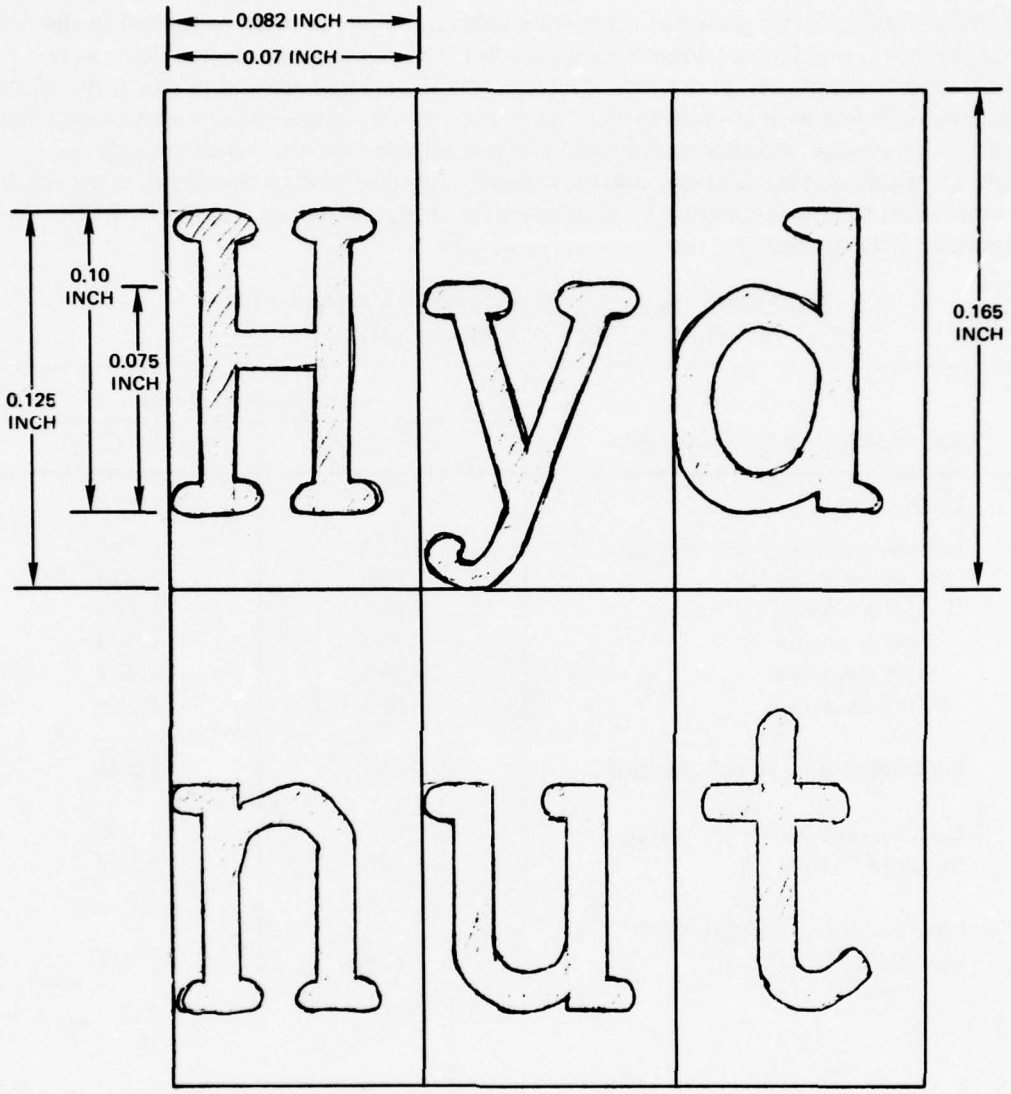
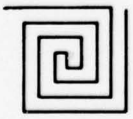
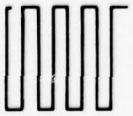


Figure D7. Double-spiral meander.





+6x, –6y, –5x, +4y, +3x, –2y, –1x, +1y, –1x
-2y, +3x, +4y, –5x, –6y, +7x, +7y
CHECK: $\Sigma y = 0$ LENGTH = 63
$\Sigma x = 7$



+0x, -ny, +1x, +ny
$0 \leq n \leq 7$
LENGTH = 2n + 1

Figure D8. Meander patterns for compression studies.

RESULTS

ILLUMINATION CORRECTION

Table D1 compares compression ratios calculated on the same image that was illumination corrected using several different calibration curves. These are to be compared to the first entry in the table, which is the compression ratio for the uncorrected image. There were three different types of corrections run. The first was the normal method in which the white standard was scanned with the lens focused on it and 16 lines of the image were summed and averaged. This average was then computed by use of different bit precisions; namely, 6 through 10. Each of these calibration curves was then used to correct the image, after which the compression ratio was computed. In all cases the compression ratios for both RLC codes are significantly lower than for the uncorrected image.

TABLE D1. COMPRESSION RATIO VS TYPE OF ILLUMINATION CORRECTION.

Type of Illumination Correction	Compression Ratio	
	2-bit Code	3-bit Code
Uncorrected		
Lens focused on white standard	1.759	1.565
6-bit precision	1.579	1.384
7-bit precision	1.602	1.407
8-bit precision	1.596	1.403
9-bit precision	1.595	1.401
10-bit precision	1.592	1.399
Lens defocused 10-bit precision	1.562	1.381
Lens focused 10-bit precision smoothed–3-pel avg	1.615	1.433
Lens focused 10-bit precision smoothed–11-pel avg	1.639	1.465

The second type of correction run was done by using a calibration curve obtained with the lens defocused in an attempt to minimize the introduction of artifacts from the white standard that are not averaged out when the 16 lines are summed together. This produced an even lower compression ratio. No explanation for this has been found.

The third type of correction was done after smoothing the 10-bit calibration curve used for the first test. Two degrees of smoothing were used, a 3-pel average and an 11-pel average. The compression ratio obtained with the 11-pel average was the highest of all the tests.

From these tests, it is believed that the $BaSO_4$ white standard and system noise together contribute enough artifacts to the calibration curve that they override any small pel-to-pel nonlinearities which the illumination correction procedure was designed to compensate for. If this is indeed true, then smoothing the calibration curve will have the effect of introducing the least amount of additional noise into the corrected image.

Upon analyzing the total number of runs in each of the bit planes in the uncorrected and the corrected image using 11-pel averaging, the reason for the lower compression ratio was found. It was found that the average brightness of the background, both before and after correction, was about level 47 or 48. This is the point at which there is a 5-bit turnover; ie, level 47 decimal is 101111 binary and 48 is 110000 binary. The correction procedure raises the pel values at the edges of the page to the levels in the center, causing more values to be around 47 and 48. With the increased number of transitions in bit plane five there was a resultant increase in the number of runs for that bit plane which in turn reduced the compression ratio for that image. This conclusion is supported by the fact that for other images with the average background brightness at a different level, the compression ratio did increase after illumination correction.

MEANDER STATISTICS

This section presents a relatively large volume of data in a highly condensed form. These data represent several tradeoff studies run on a very few image samples. It is hoped, however, that the results obtained will show valid trends for the image types studied. It is further hoped that sufficient data may be gathered at a later date to substantiate these results.

RUN LENGTH STATISTICS

For several of the images analyzed for this report, the analyses were done for both binary and Gray codes. Figures D9 and D10 present run length statistics for the typed page in binary and Gray code, respectively. Since Gray code exhibits fewer transitions, level to level, than binary code, there should significantly more longer runs of 1's or 0's in each of the bit planes except the most-significant bit plane, which is identical in binary and Gray. In comparing figures D9 and D10 it can easily be seen in at least the first three bit plane diagrams that there are more entries at longer run lengths in figure D10 than in figure D9. The compression ratio calculation for this image is about 35% greater in Gray code than in binary.

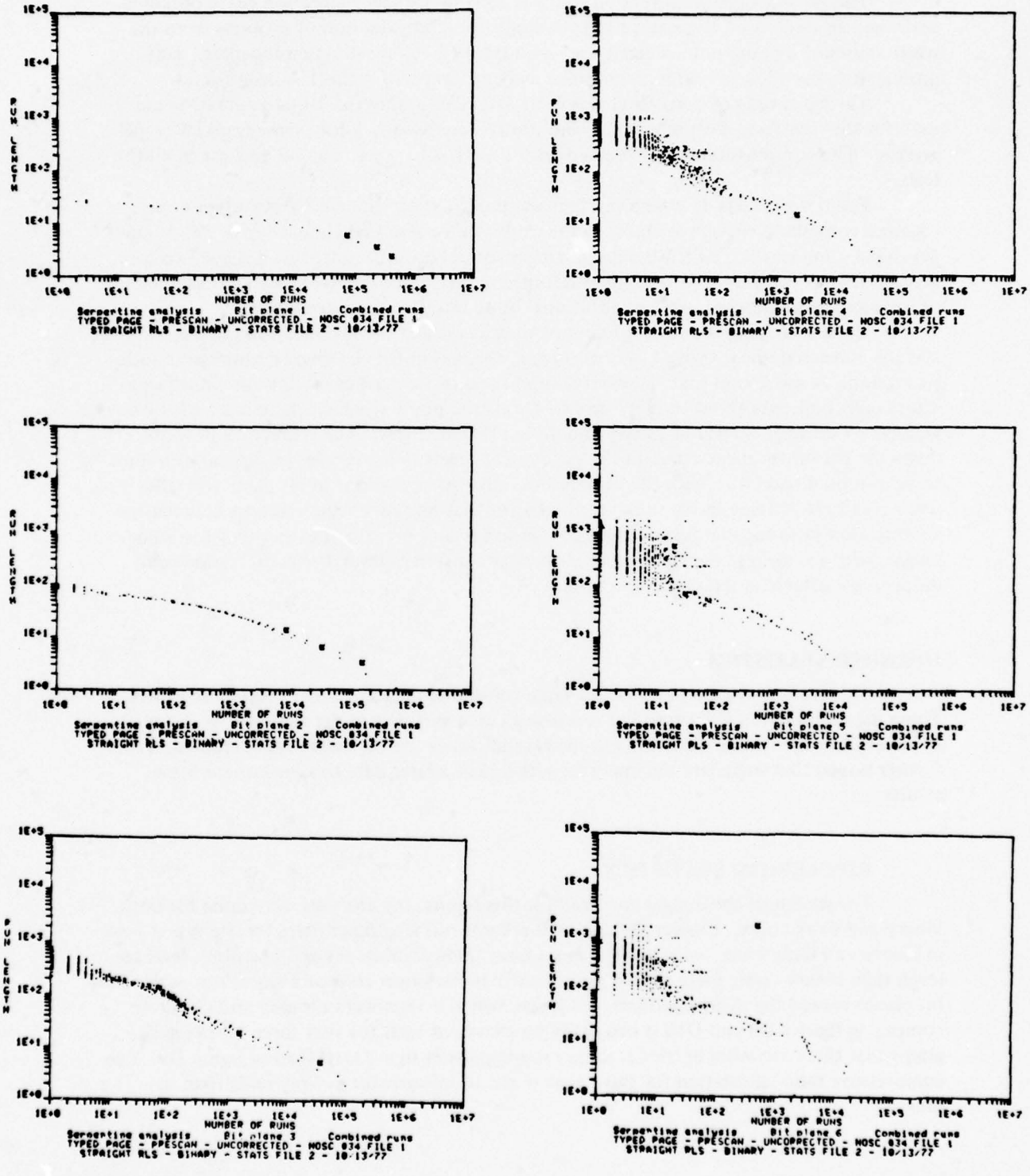


Figure D9. Run length statistics.

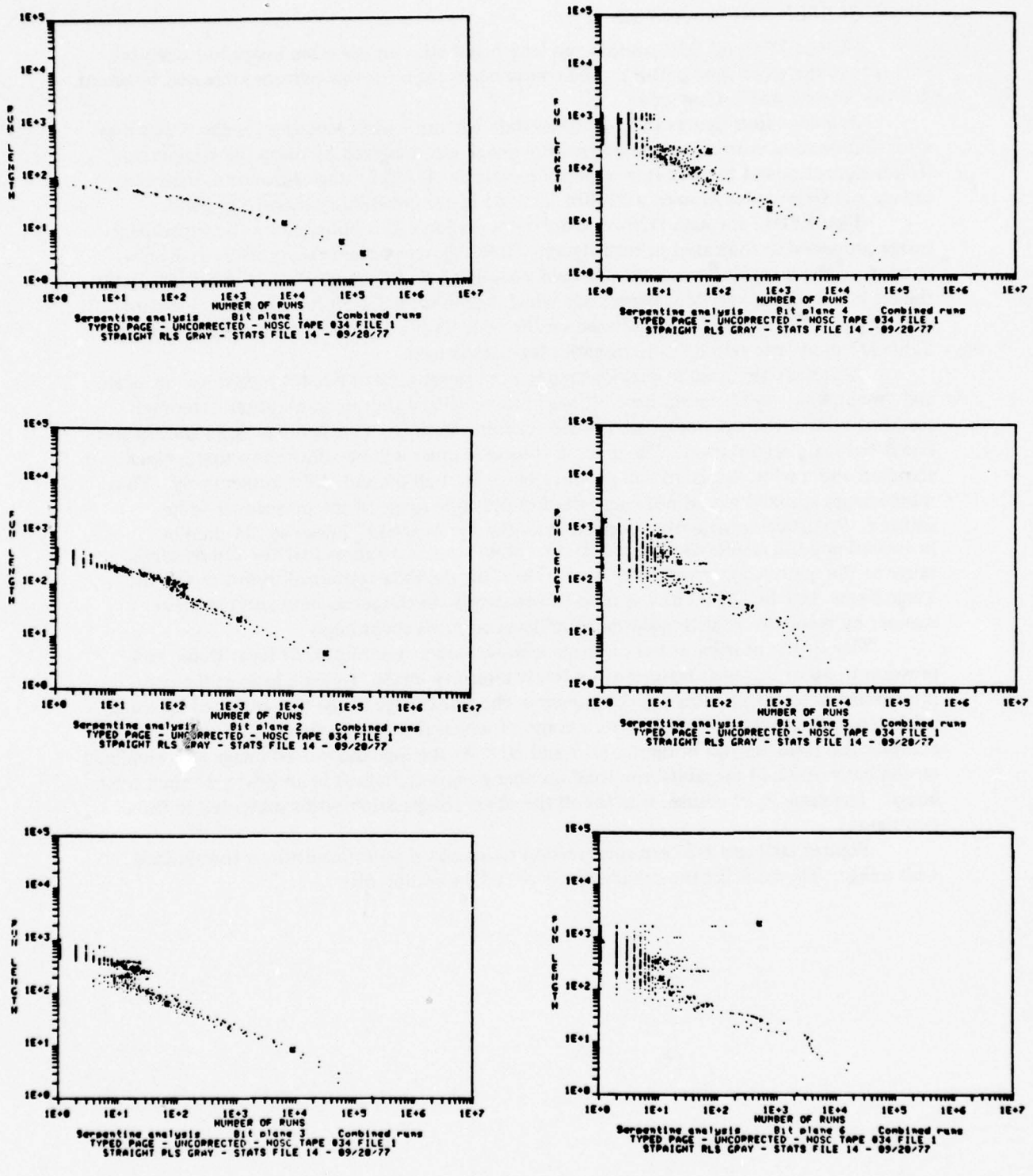


Figure D10. Run length statistics.

SERPENTINE ANALYSIS

Figures D11 and D12 contain run length statistics on the same image but analyzed with a two-line serpentine pattern. The compression ratio for this pattern increased by about 40% when analyzed in Gray code.

The next four figures (D13-D16) contain the run length statistics for the typed page after illumination correction. As before, the image was analyzed by using the straight run length algorithm and the two-line serpentine pattern. The resulting comparison between binary and Gray codes showed a 30-40% increase in compressibility with Gray code.

Figures D17 through D20 compare compression ratios obtained on the typed page image processed as indicated in each figure. These figures contain compression ratios calculated on the 6-bit image as if all 6-bit planes were to be transmitted. Figure D17 contains figures based on the variable-length code which begins with a 2-bit minimum code length while figure D18 contains figures based on the code with a 3-bit minimum code length. Table D2 shows the two RLC dictionaries for comparison.

Although discussed in previous reports, a brief review of what is meant by "prescan" and "main scan" will be given here. It has been visualized that in an eventual letter mail scanning system there actually will be two scanning stations. One is the prescan station and one is the main scan station. The prescan station scanner will be adjusted so that a black standard and a white standard will produce outputs of all 0's and all 1's, respectively. Thus, most images scanned would not cause the full dynamic range of the prescanner to be utilized. Statistical information derived from the "prescanned" image would then be processed and the results used to set up the "main scan" station so that the full dynamic range of the main scanner would be used. Thus, for the data contained in this report the Large Drum Test Bed (LDTB) was used to simulate both the prescanner and the main scanner by manually adjusting the gain and level controls accordingly.

One of the possible types of image compression is a nonlinear or logarithmic compression to 16 or 32 levels instead of 64 linear intensity levels. To get a look at the compressibility of an image using log compression, the typed page image was analyzed by using a 5-bit log compression look-up table, a graph of which is shown in figure D21. The compression ratios shown in figures D17 and D18 for the log-compressed image are calculated on the basis of 22.44 megabits, the total number of bits contained in an 8½-by-11-inch 6-bit image. The same is, of course, true for all the other compression ratios presented in those two figures.

Figures D19 and D20 are compression ratios based on transmitting a thresholded 1-bit image. The basis for the calculation here is 3.74 million bits.

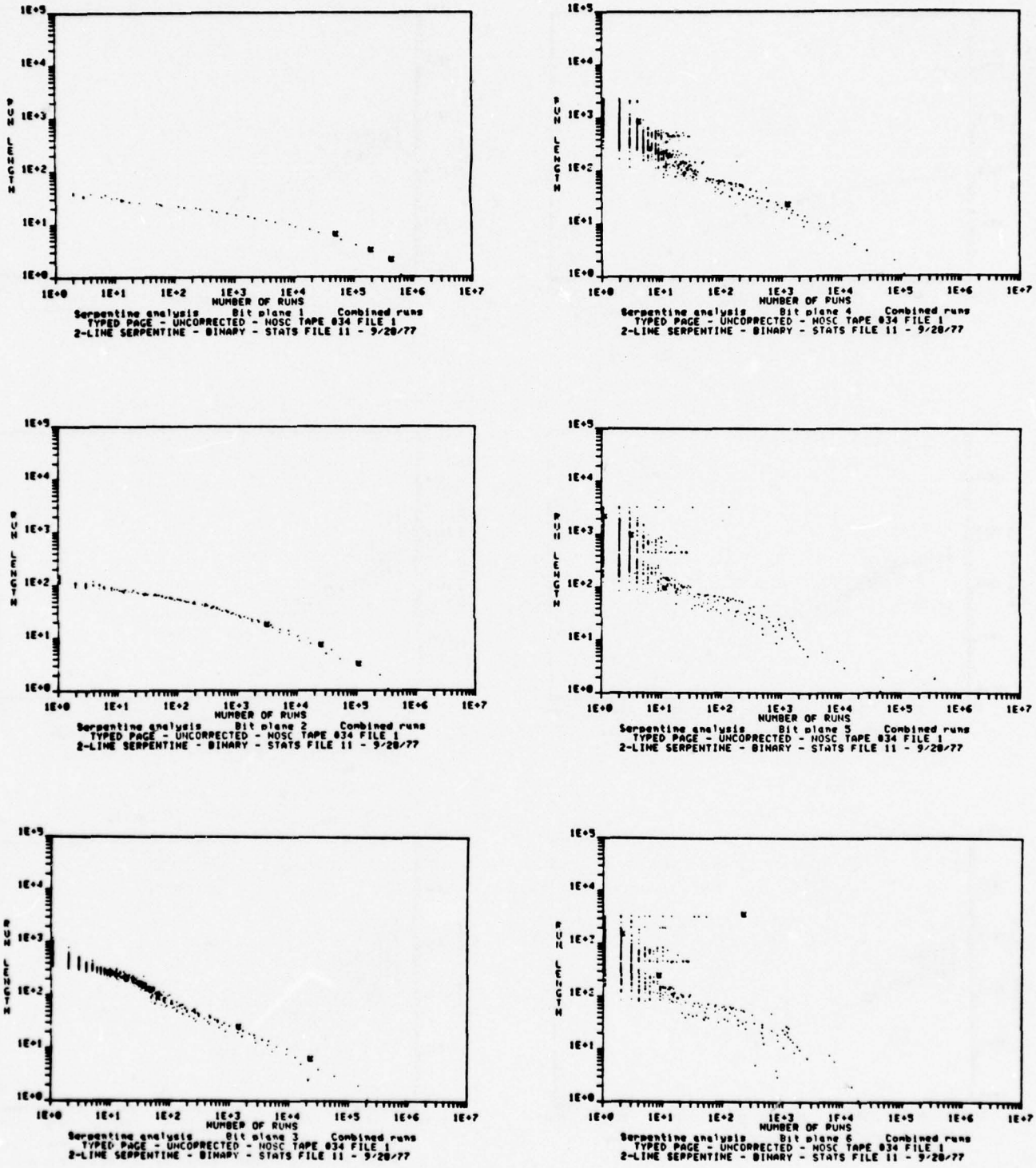


Figure D11. Run length statistics.

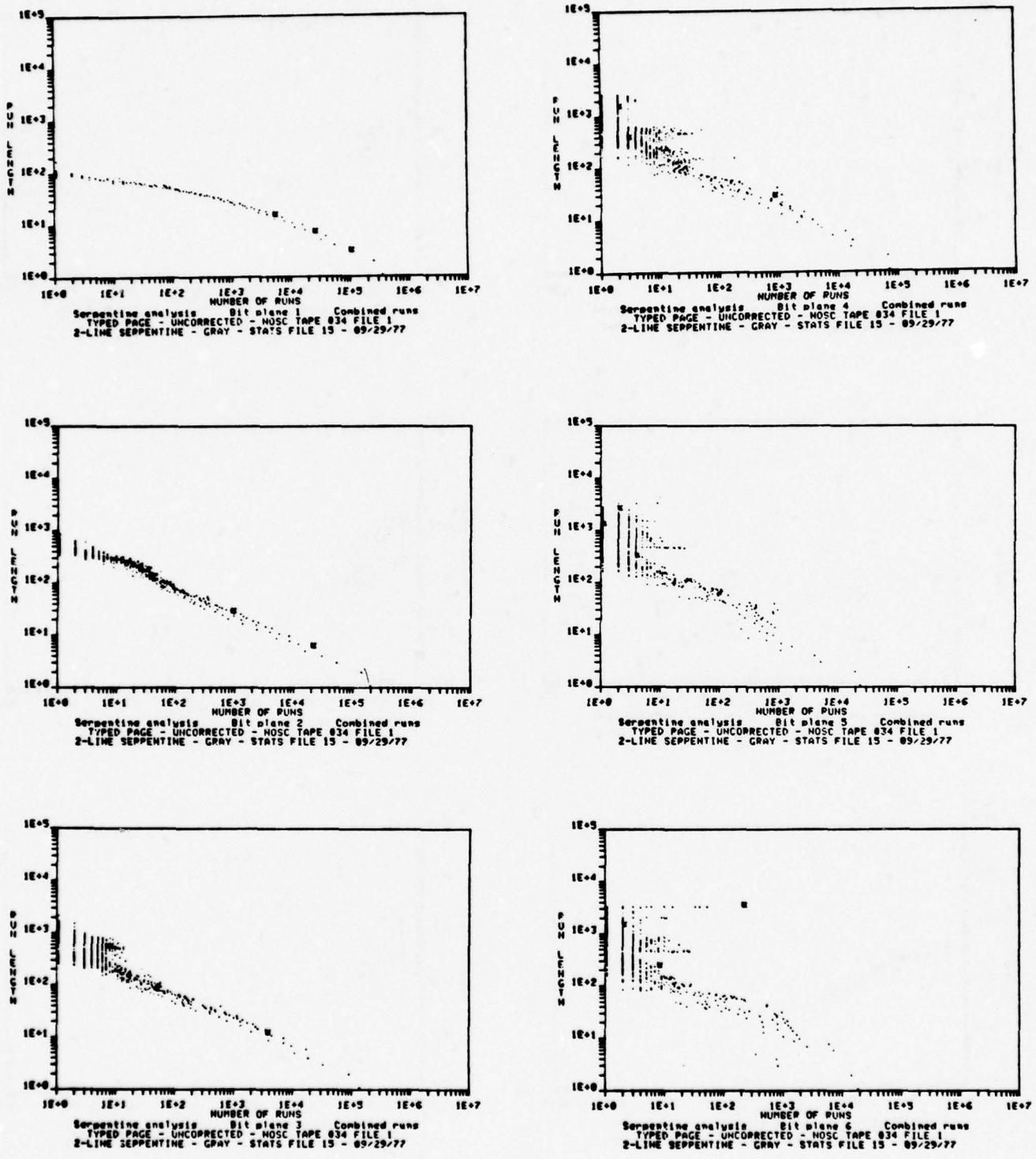


Figure D12. Run length statistics.

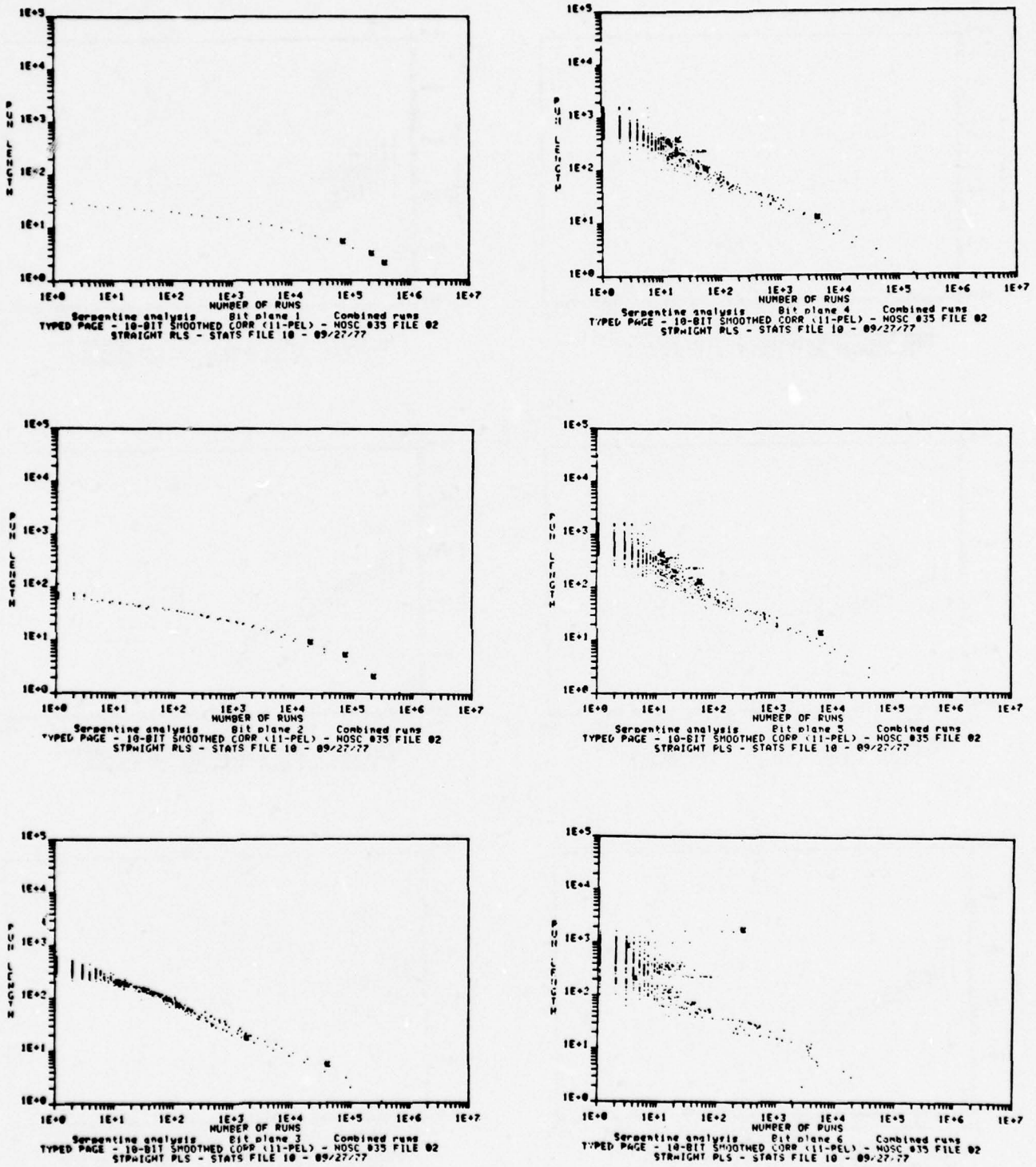


Figure D13. Run length statistics.

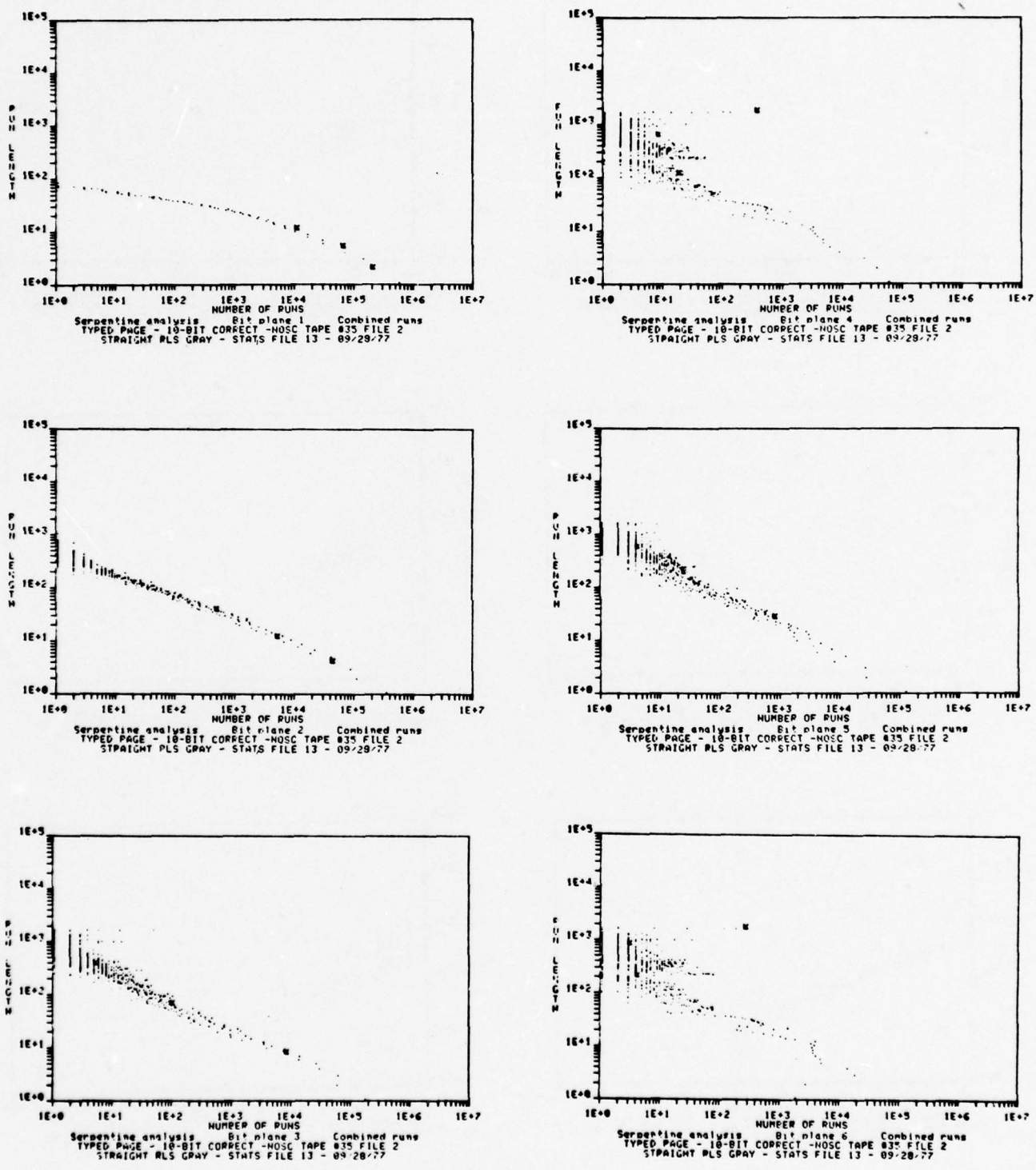


Figure D14. Run length statistics.

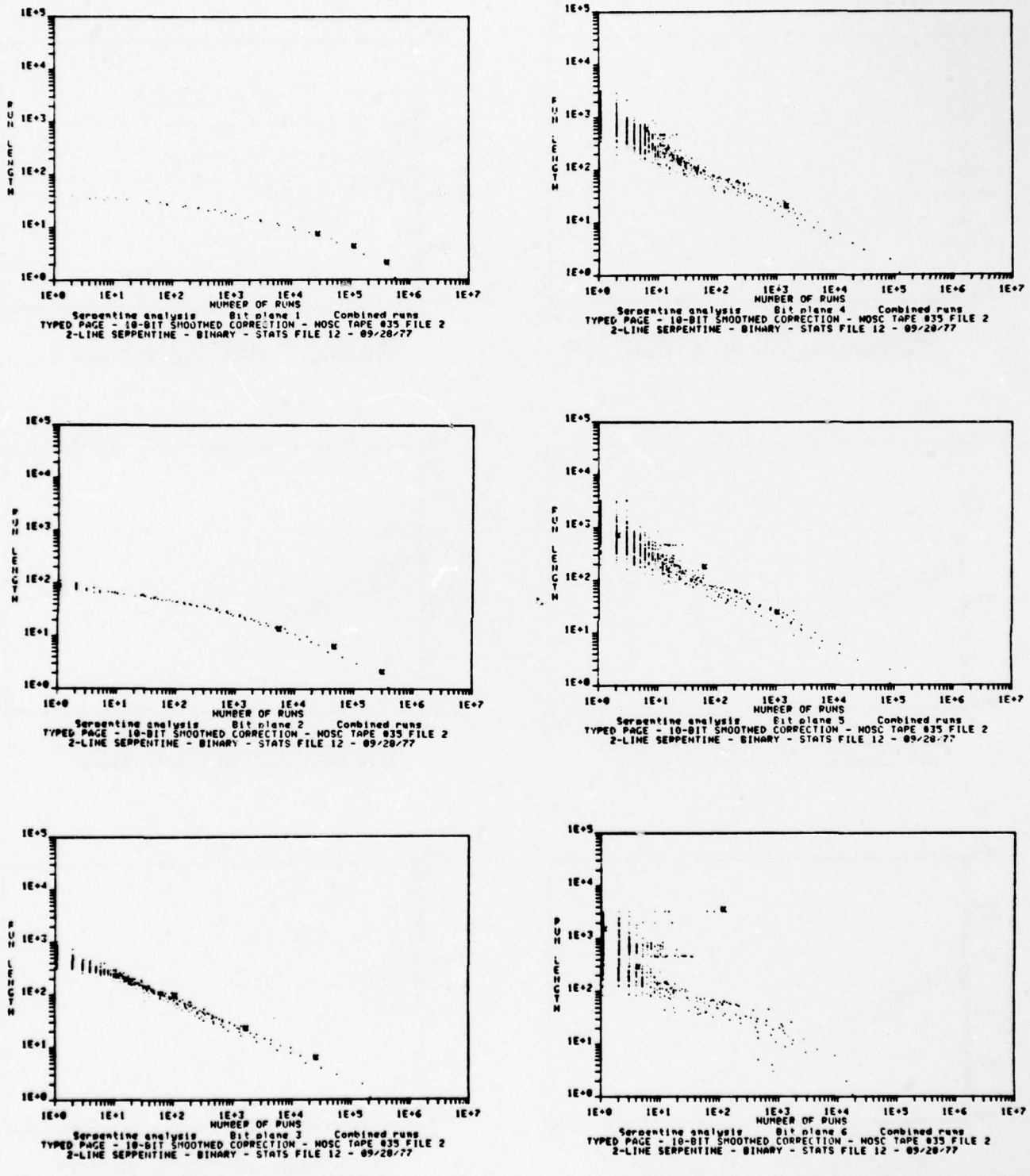


Figure D15. Run length statistics.

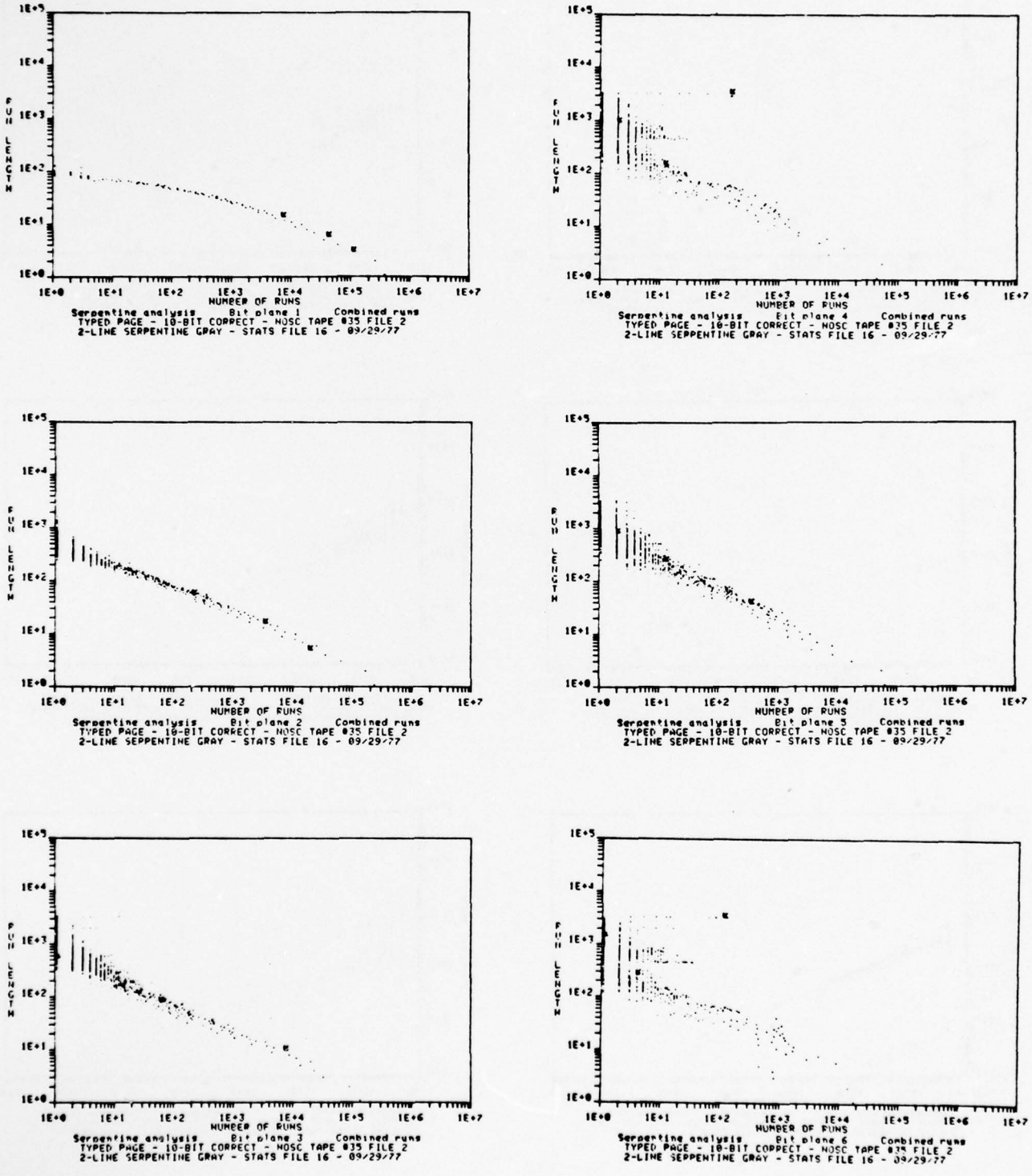


Figure D16. Run length statistics.

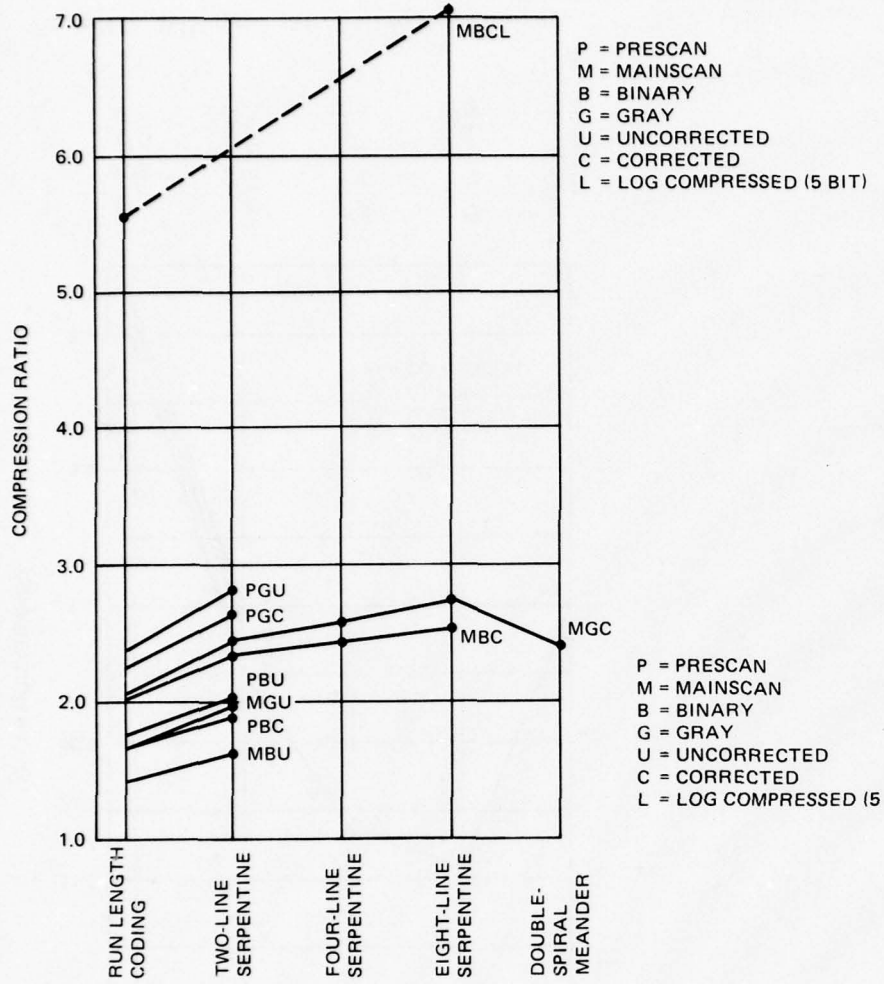


Figure D17. WJM typed paged, 2-bit coding.

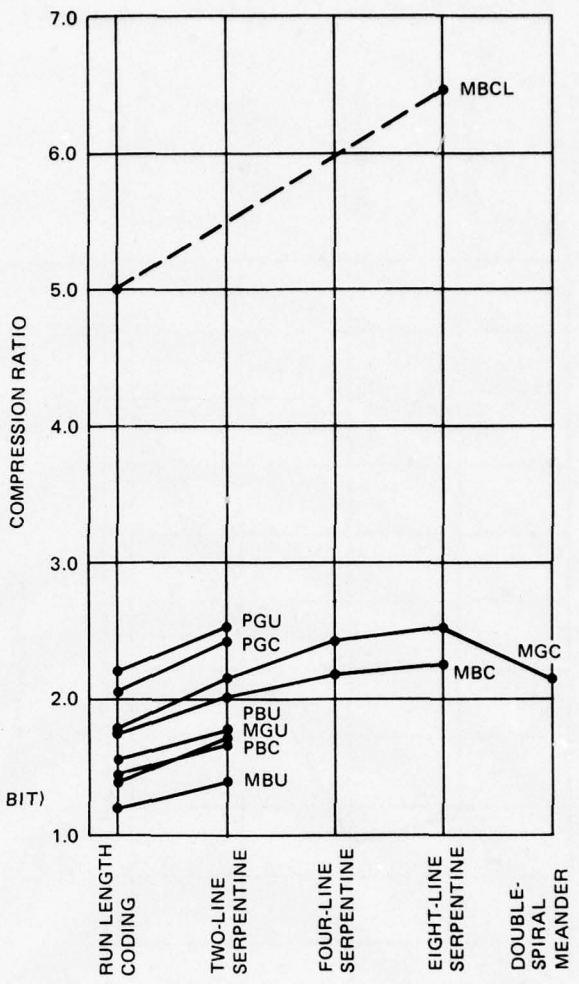


Figure D18. WJM typed page, 3-bit coding.

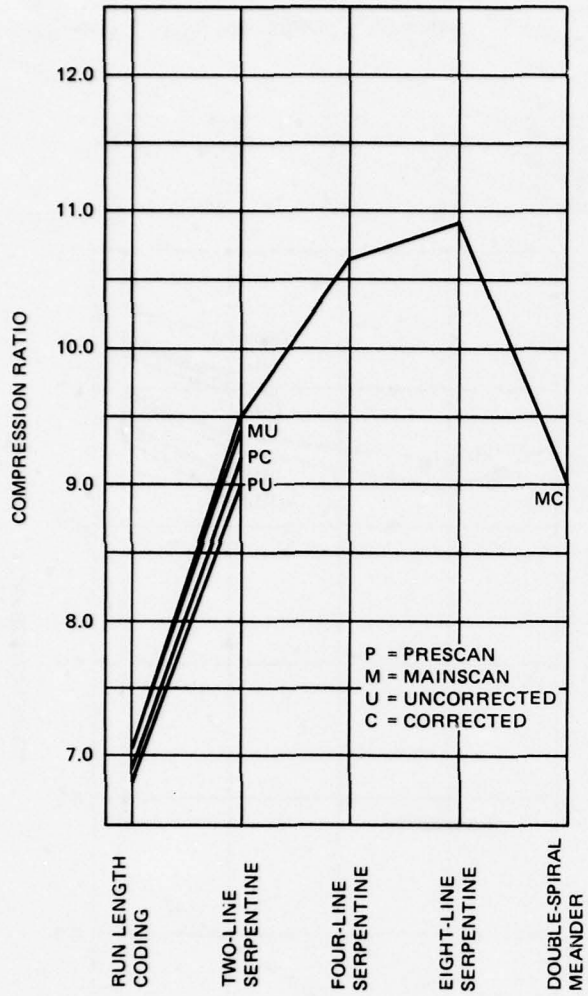


Figure D19. WJM typed page, 2-bit coding, MSB only.

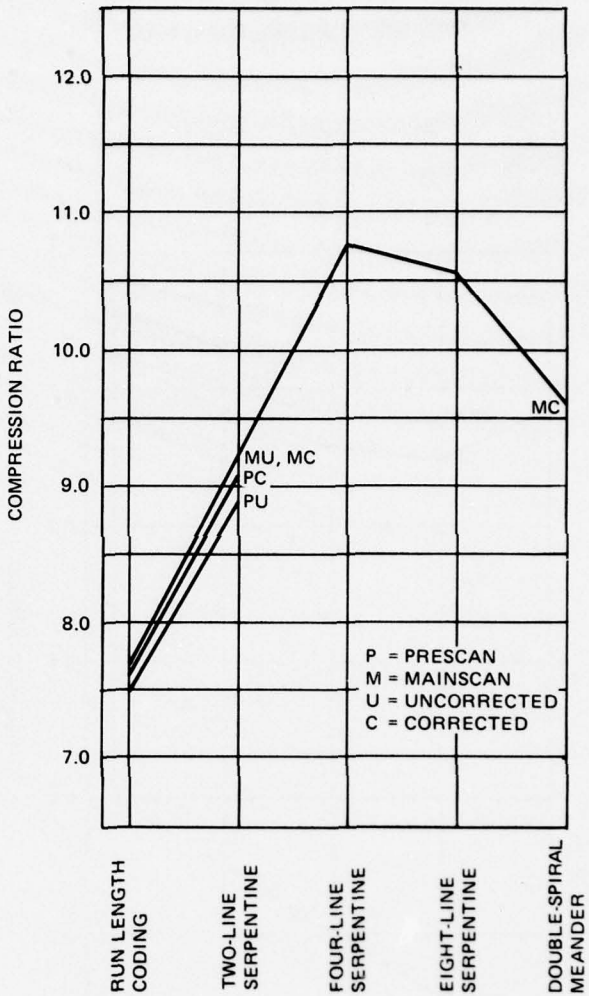


Figure D20. WJM typed page, 3-bit coding, MSB only.

TABLE D2. VARIABLE-LENGTH RUN LENGTH DICTIONARIES.

2-Bit Code		3-Bit Code	
Run Length	Word Length	Run Length	Word Length
1–2	2	1–4	3
3–6	4	5–8	4
7–14	6	9–16	6
15–30	8	17–32	8
31–62	10	33–64	10
63–126	12	65–128	12
127–254	14	129–256	14
255–510	16	257–512	16
511–1022	18	513–1024	18
1023–2046	20	1025–2048	20
2047–4094	22	2049–4096	22
4095–8190	24	4097–8192	24
8191–16382	26	8193–16384	26

Figures D22 through D25 are run length statistics on the RCA "S" image, an image containing fine typing and fine graphics. The statistics are shown for straight RLC and 2-, 4-, and 8-line serpentine patterns. When comparing these statistics against each other for the different patterns, it is difficult to see much change in the lower bit planes, as could be seen in earlier figures for the typed page image. Here, the significant changes appear to be in the higher-order bit planes.

Figures D26 and D27 are summaries of the compression ratios for the "S" image, both for a 6-bit image and a thresholded or 1-bit image.

A compression ratio summary for a continuous-tone image is shown in figure D28.

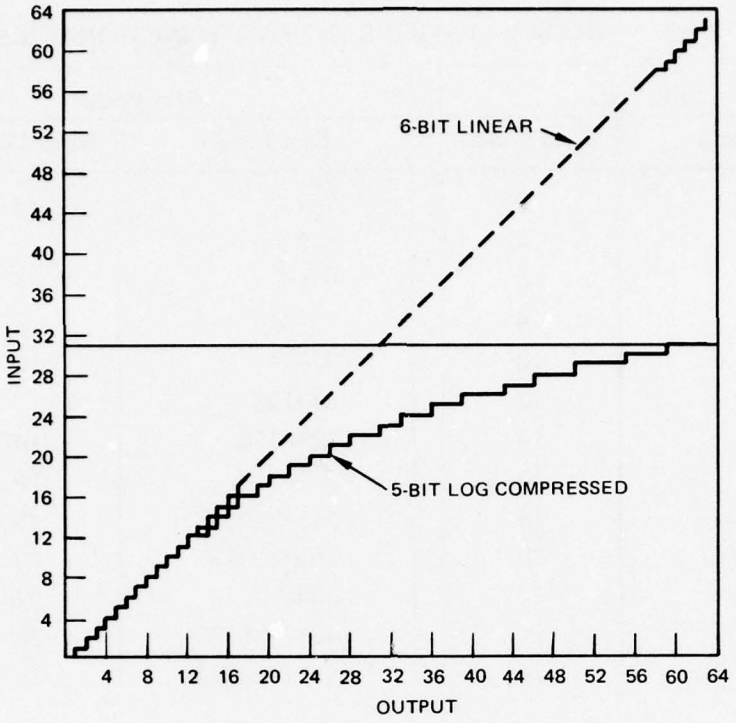


Figure D21. Non-linear five-bit image compression.

DOUBLE-SPIRAL STATISTICS

In comparing figures D17 through D28, several observations may be made. The two-line serpentine algorithm shows a definite improvement over the straight run length algorithm. For the images on which the four-line and eight-line analyses were run the four-line was better than the two-line algorithm and in all but one case the eight-line algorithm was better than the four-line. However, the complex double-spiral meander pattern proved somewhat less desirable than certain serpentine patterns. In comparing compression ratios for 6-bit images, the continuous-tone image appears to have a higher overall compressibility than a primarily bilevel image analyzed as a 6-bit image.

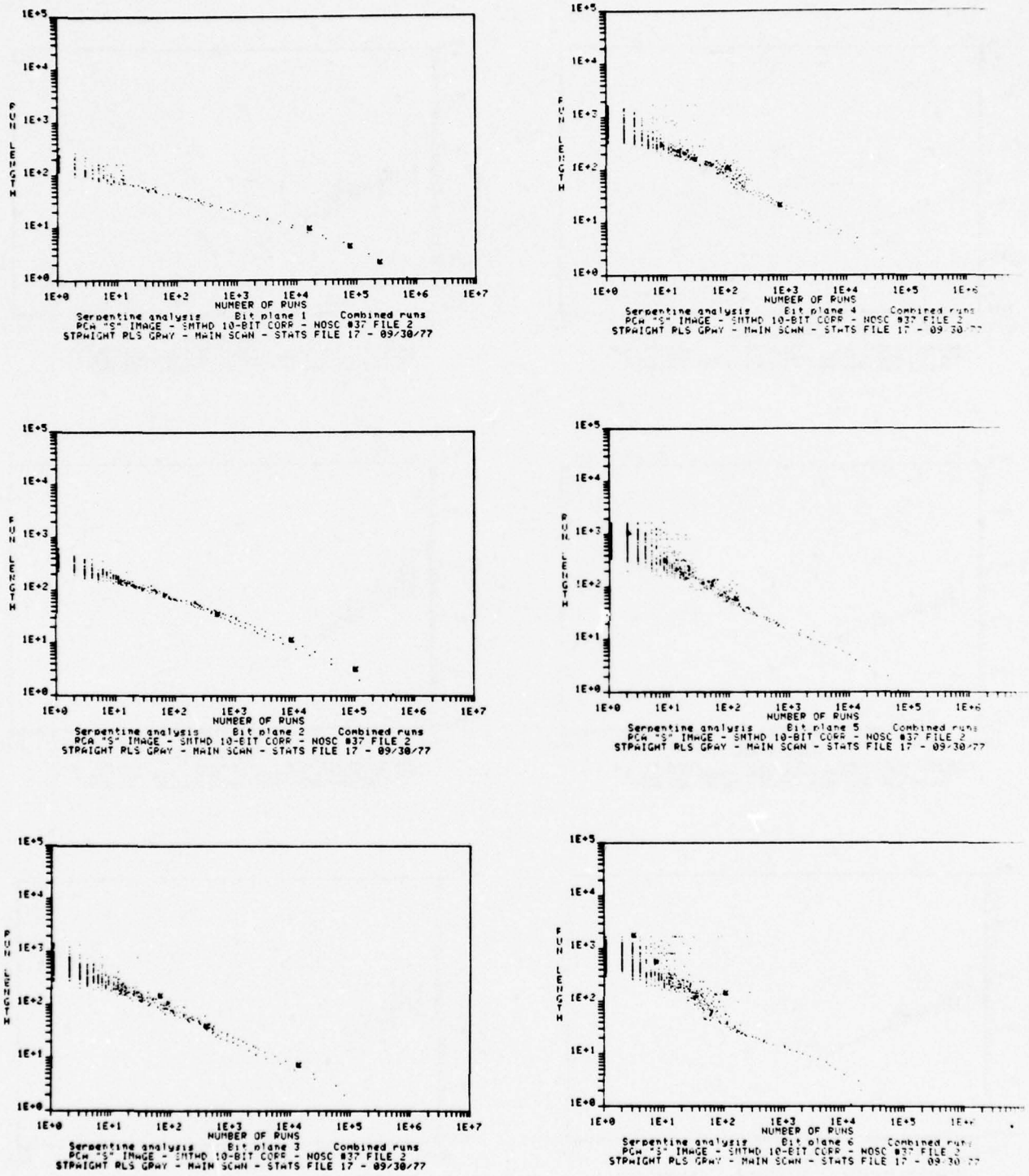


Figure D22. Run length statistics.

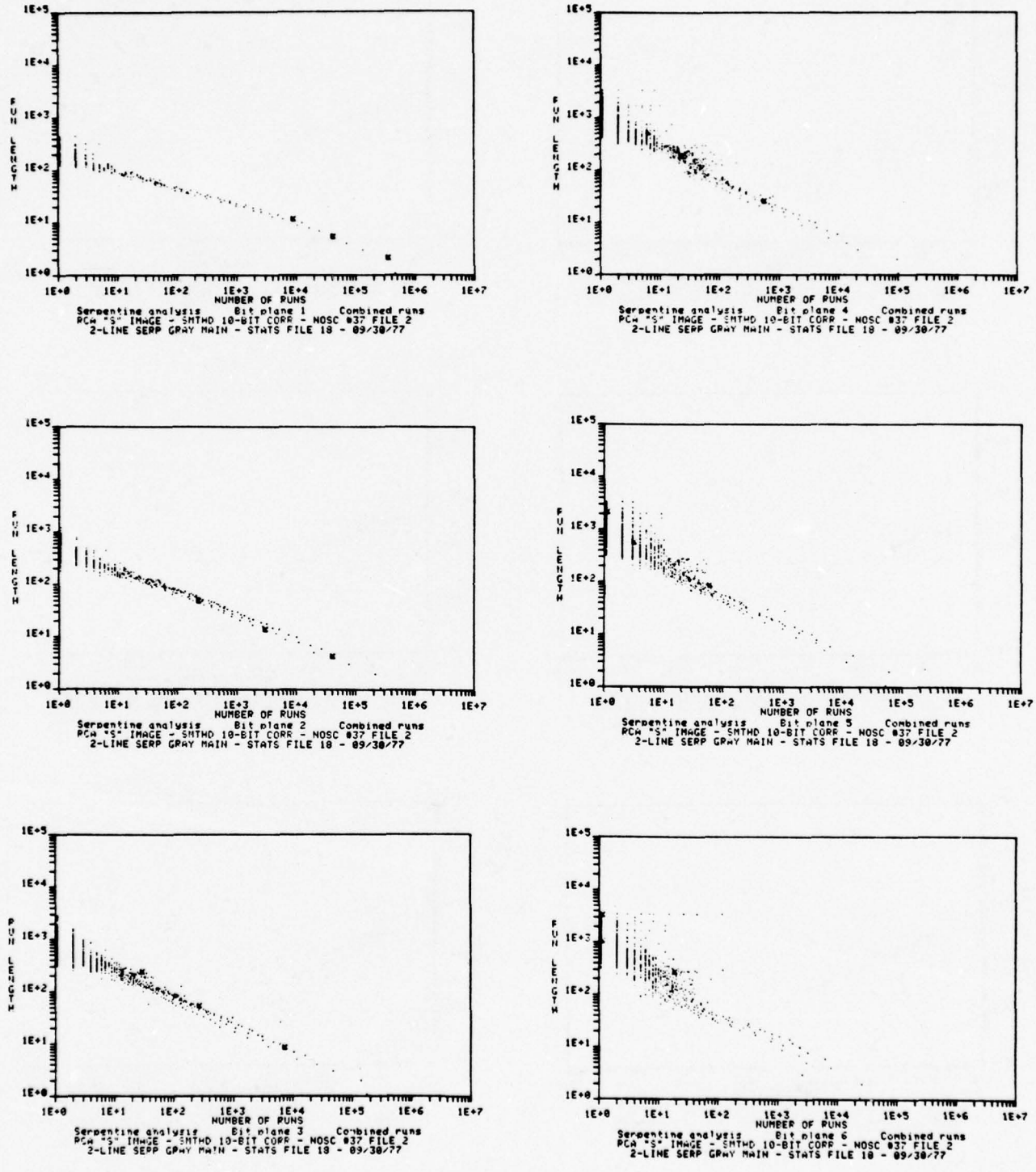


Figure D23. Run length statistics.

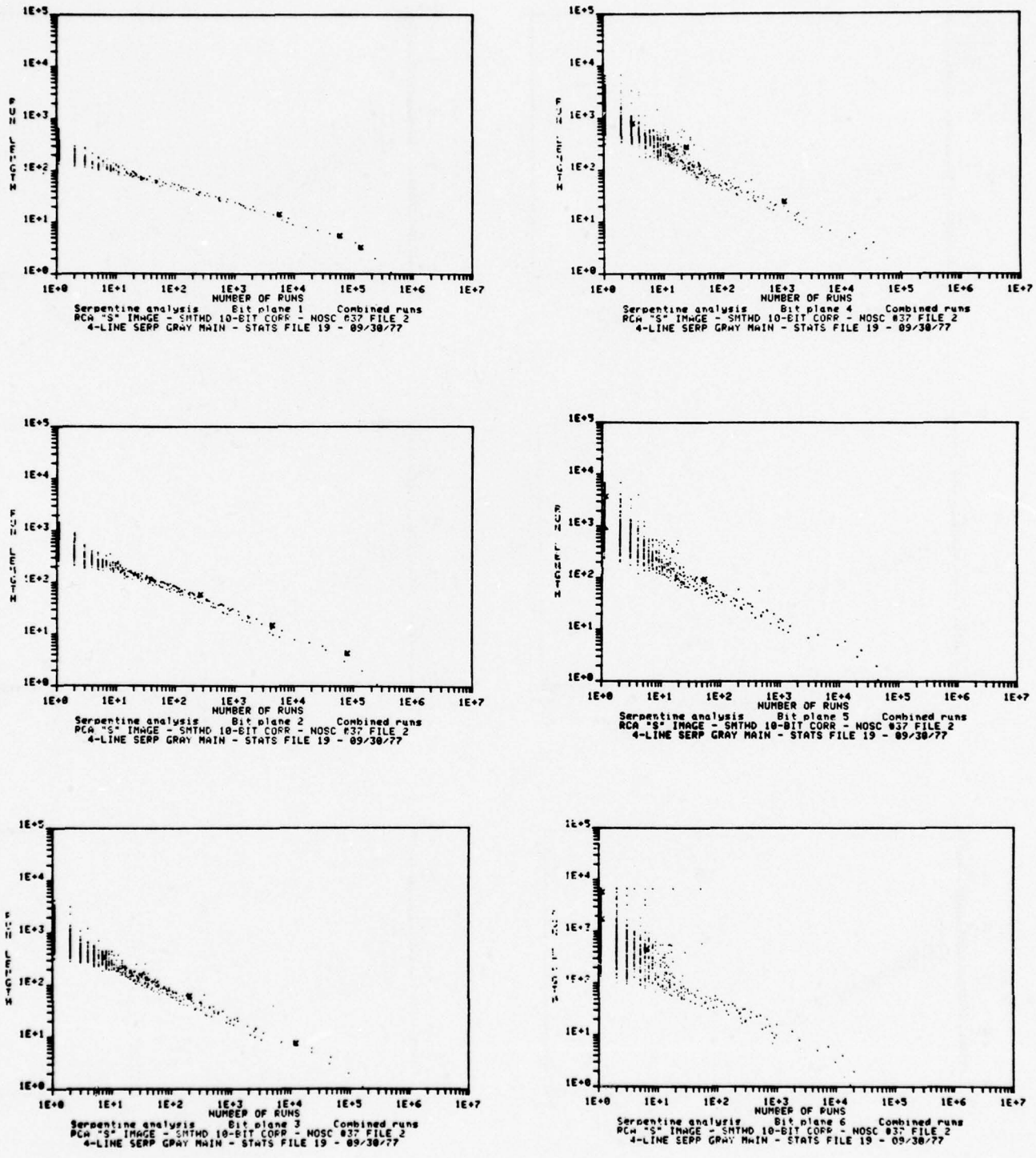


Figure D24. Run length statistics.

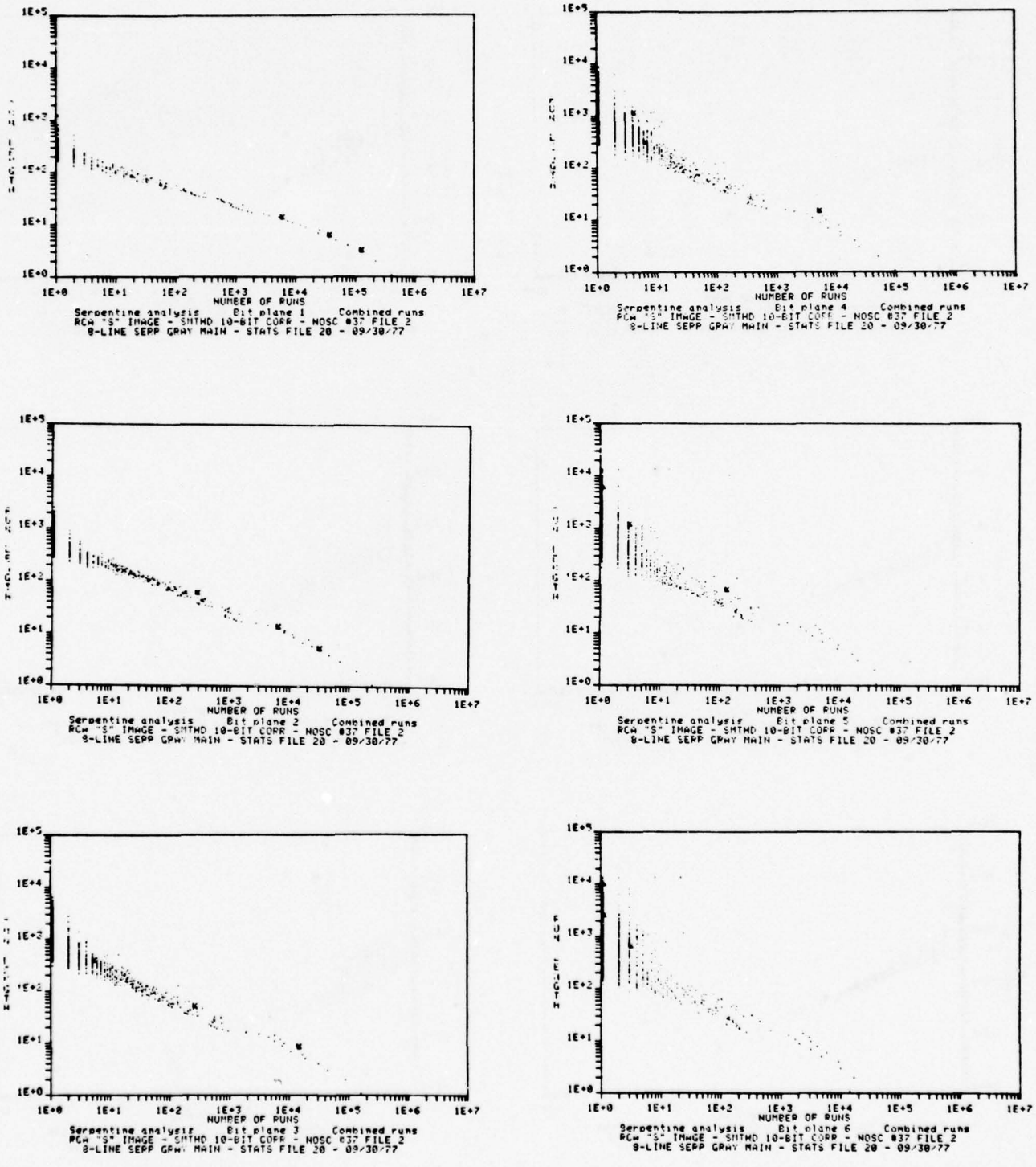


Figure D25. Run length statistics.

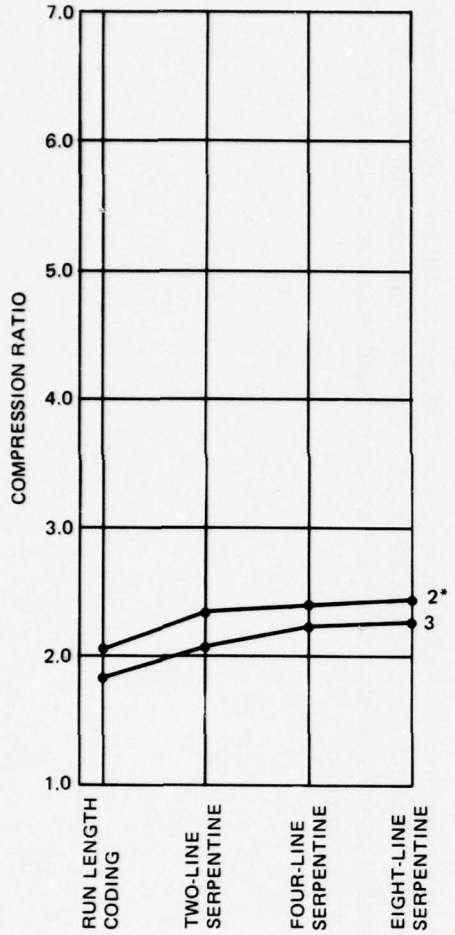


Figure D26. RCA "S" image.

*Main scan Gray code, corrected
2 = 2-bit code 3 = 3-bit code

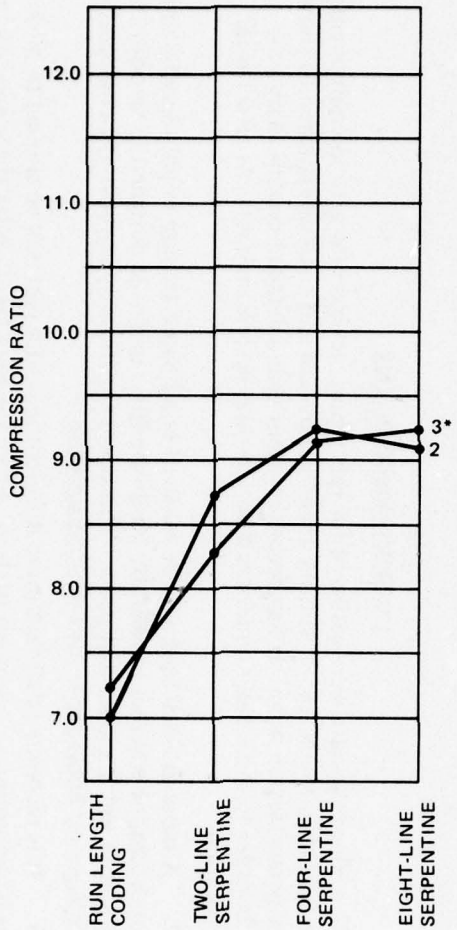


Figure D27. RCA "S" image, MSB only.

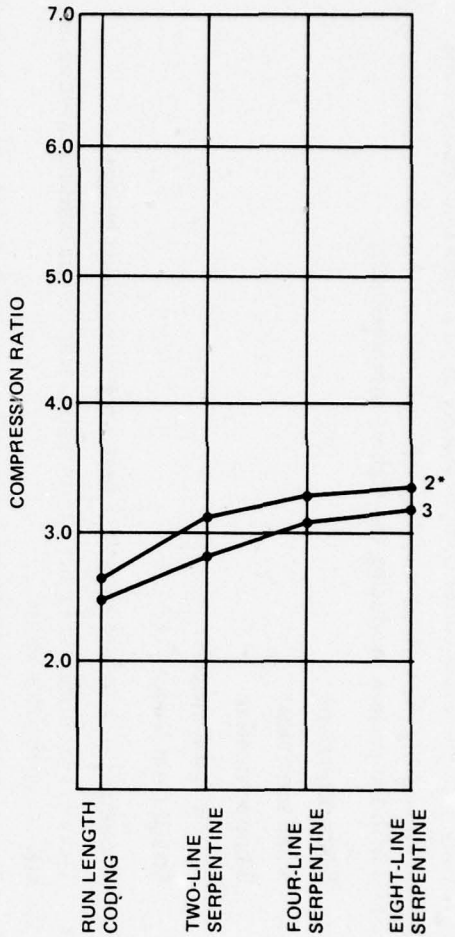


Figure D28. Continuous tone image.

CONCLUSIONS

1. Gray code produces better compressibility in all images than binary code.

2. In comparing the various encoding schemes, the order of compressibility appears to be, starting with the pattern producing the highest compressibility:

   8-line serpentine

   4-line serpentine

   2-line serpentine

   Double-spiral meander

   Straight run length

3. Compression ratios are about 5:1 better for thresholded images.

4. There is a significantly higher compression ratio for the continuous-tone image than for the bilevel typewritten image.

5. The nonlinear, or logarithmic, compression produced much higher compression ratios when run length or meander encoded than did the linear 6-bit images.

FUTURE NOSC PLANS

1. Since the data were gathered for this report, several new system components have been added to the ICAS. Resulting image acquisition and analysis appeared to show significantly less system noise. It has become evident that a detailed system analysis is required in order to more fully understand how various system components affect total system operation.

2. A more detailed look will be taken at bond paper texture vs photographic paper texture to determine whether a realizable hardware filter might be designed to smooth the paper texture found in most bond paper. This could significantly improve the compressibility of images on bond paper for 6-bit transmission.

3. It is recommended that more different meander patterns be studied to more conclusively determine an optimum pattern. From the data taken so far there appears to be an optimum between the four-line serpentine and the eight-line serpentine patterns.

4. A closer look at the $BaSO_4$ white standard used to calibrate the ICAS revealed the undesriable characteristic of being very rough in texture. It appears that white photographic quality paper has a much more uniform texture and would be a much better target to scan as a white standard.

ANNEX A: INDIVIDUAL RUN LENGTH VALUES FOR UNCORRECTED PRESCAN BINARY RLS

LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
1	825928	32	1				
2	377775						
3	218483						
4	113785						
5	60352						
6	36554						
7	22728						
8	12730						
9	8044						
10	4783						
11	3031						
12	1859						
13	1207						
14	723						
15	486						
16	320						
17	226						
18	135						
19	99						
20	50						
21	37						
22	38						
23	18						
24	13						
25	3						
26	3						
27	2						
28	3						

Serpentine analysis Bit plane 1 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
STRAIGHT RLS - BINARY - STATS FILE 2 - 10/13/77

LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
1	542334	29	702	57	25	86	2
2	165666	30	714	58	31	87	3
3	134796	31	570	59	20	92	2
4	61598	32	531	60	20	93	1
5	59787	33	453	61	12	94	1
6	28164	34	419	62	15	95	1
7	29880	35	361	63	14	99	1
8	15723	36	323	64	7	100	2
9	16640	37	284	65	3		
10	9176	38	274	66	17		
11	10368	39	250	67	6		
12	6441	40	231	68	6		
13	7075	41	178	69	6		
14	4395	42	172	70	7		
15	4682	43	131	71	5		
16	3333	44	138	72	6		
17	3695	45	97	73	2		
18	2572	46	88	74	2		
19	2732	47	90	75	3		
20	2074	48	96	76	4		
21	2060	49	68	77	3		
22	1727	50	90	78	4		
23	1535	51	48	80	2		
24	1301	52	62	81	2		
25	1205	53	34	82	1		
26	921	54	41	83	1		
27	909	55	39	84	1		
28	754	56	36	85	1		

Serpentine analysis Bit plane 2 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
STRAIGHT RLS - BINARY - STATS FILE 2 - 10/13/77

LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
1	327165	29	768	57	261	85	109
2	97632	30	381	58	254	86	148
3	74511	31	605	59	194	87	111
4	32952	32	329	60	167	88	122
5	33969	33	641	61	169	89	98
6	15819	34	290	62	159	90	113
7	17882	35	481	63	192	91	104
8	9648	36	277	64	139	92	133
9	10579	37	477	65	183	93	103
10	5153	38	205	66	149	94	87
11	7201	39	416	67	169	95	79
12	4474	40	197	68	192	96	87
13	5435	41	329	69	152	97	100
14	2745	42	179	70	171	98	99
15	3362	43	282	71	152	99	104
16	1696	44	189	72	185	100	97
17	2748	45	289	73	149	101	77
18	1502	46	214	74	137	102	96
19	2035	47	295	75	153	103	78
20	1061	48	188	76	137	104	86
21	1643	49	304	77	151	105	54
22	926	50	153	78	119	106	86
23	1234	51	335	79	141	107	76
24	623	52	218	80	130	108	99
25	1101	53	258	81	104	109	59
26	684	54	196	82	133	110	75
27	1137	55	215	83	194	111	79
28	546	56	151	84	126	112	83

Serpentine analysis Bit plane 3 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
113	49	141	36	169	21	197	6
114	82	142	48	170	32	198	15
115	63	143	37	171	11	199	11
116	101	144	75	172	27	200	10
117	48	145	43	173	14	201	6
118	85	146	69	174	27	202	8
119	59	147	38	175	11	203	5
120	72	148	64	176	24	204	12
121	47	149	31	177	18	205	5
122	61	150	47	178	18	206	5
123	57	151	24	179	9	207	4
124	82	152	50	180	19	208	8
125	56	153	20	181	9	209	4
126	66	154	36	182	18	210	11
127	41	155	24	183	13	211	1
128	75	156	57	184	15	212	15
129	39	157	25	185	16	213	4
130	71	158	38	186	16	214	9
131	43	159	25	187	10	215	7
132	53	160	49	188	15	216	15
133	35	161	15	189	5	217	4
134	73	162	24	190	14	218	10
135	50	163	17	191	12	219	1
136	62	164	44	192	11	220	7
137	47	165	26	193	8	221	4
138	65	166	37	194	13	222	13
139	35	167	19	195	9	223	9
140	75	168	28	196	19	224	10

Serpentine analysis Bit plane 3 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
225	5	253	4	283	6	313	3
226	10	254	3	284	2	315	3
227	3	256	7	285	3	316	1
229	10	257	4	286	1	317	1
229	5	258	3	287	1	318	2
230	4	259	1	288	5	319	1
231	7	260	3	289	3	320	1
232	4	261	3	290	3	321	1
233	5	262	7	291	1	322	1
234	5	263	4	292	2	323	1
235	4	264	2	293	2	324	2
236	9	265	2	294	1	325	1
237	4	266	1	295	3	326	2
238	5	267	2	296	1	327	2
239	5	268	4	297	1	328	1
240	8	269	7	298	1	331	2
241	8	270	3	299	1	332	2
242	4	271	6	300	2	333	1
243	6	272	4	301	4	336	4
244	4	273	3	302	3	337	2
245	3	274	5	303	7	338	3
246	6	275	3	304	1	339	1
247	5	276	5	305	1	340	1
248	4	277	2	307	4	342	2
249	10	278	2	308	1	343	1
250	2	279	3	309	1	345	1
251	4	280	6	310	3	346	1
252	1	282	1	311	3	347	1

Serpentine analysis Bit plane 3 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
348	1	394	1	440	2	488	1
349	1	395	3	441	1	481	1
351	1	397	2	443	1	483	2
352	2	398	3	446	1	488	2
353	2	399	1	449	1	490	1
354	1	401	3	450	1	491	2
359	5	406	1	451	4	492	1
361	2	407	1	453	2	493	2
363	3	408	2	454	3	494	1
364	1	409	1	455	1	496	1
369	1	410	1	458	1	497	1
369	2	412	1	459	1	499	2
370	2	413	2	461	1	500	1
372	2	414	4	462	1	502	1
373	3	415	3	463	3	509	3
374	1	417	2	464	1	513	1
375	1	419	1	465	1	515	2
376	3	420	2	466	1	519	1
377	1	422	1	468	1	527	3
378	2	423	2	469	2	537	1
379	4	426	1	470	4	538	1
381	1	427	2	471	1	549	1
383	3	429	1	472	1	555	1
385	1	433	2	473	1	557	1
387	2	435	1	474	2	600	1
391	3	436	1	475	3	605	1
392	2	437	1	477	2	632	1
393	2	439	3	479	3	650	1

Serpentine analysis Bit plane 3 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
725	1						
783	1						

Serpentine analysis Bit plane 3 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
STRAIGHT RLS - BINARY - STATS FILE 2 - 10/13/77

LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
1	165791	29	630	57	106	85	25
2	51669	30	403	58	39	86	55
3	38183	31	469	59	70	87	53
4	17740	32	296	60	29	88	38
5	16751	33	388	61	66	89	32
6	8552	34	241	62	36	90	41
7	9503	35	317	63	83	91	37
8	5556	36	165	64	46	92	71
9	5929	37	244	65	97	93	59
10	3671	38	113	66	35	94	34
11	4351	39	170	67	91	95	46
12	3707	40	83	68	55	96	26
13	3205	41	115	69	62	97	61
14	2040	42	67	70	66	98	26
15	1986	43	115	71	77	99	49
16	1072	44	50	72	123	100	68
17	1356	45	118	73	98	101	27
18	753	46	89	74	44	102	75
19	891	47	126	75	115	103	46
20	370	48	90	76	413	104	34
21	1092	49	139	77	103	105	35
22	682	50	82	78	32	106	57
23	938	51	124	79	75	107	39
24	1294	52	66	80	25	108	44
25	739	53	127	81	45	109	40
26	637	54	78	82	27	110	34
27	807	55	136	83	36	111	50
28	509	56	66	84	17	112	29

Serpentine analysis Bit plane 4 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
113	43	141	15	169	16	197	8
114	50	142	5	170	11	198	13
115	34	143	20	171	19	199	10
116	43	144	20	172	9	200	8
117	45	145	15	173	40	201	11
118	25	146	17	174	23	202	49
119	49	147	17	175	20	203	30
120	73	148	15	176	16	204	19
121	53	149	31	177	19	205	11
122	27	150	11	178	9	206	9
123	50	151	27	179	7	207	8
124	25	152	21	180	22	208	10
125	28	153	16	181	22	209	15
126	41	154	13	182	37	210	8
127	41	155	17	183	14	211	8
128	19	156	16	184	8	212	11
129	34	157	17	185	7	213	9
130	24	158	10	186	12	214	13
131	36	159	13	187	11	215	20
132	17	160	8	188	14	216	22
133	31	161	12	189	8	217	28
134	24	162	17	190	10	218	2
135	18	163	26	191	15	219	9
136	16	164	25	192	50	220	5
137	14	165	17	193	10	221	7
138	7	166	12	194	10	222	12
139	29	167	13	195	15	223	12
140	13	168	11	196	12	224	8

Serpentine analysis Bit plane 4 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
225	10	253	11	281	6	309	9
226	18	254	4	282	3	310	15
227	47	255	16	283	8	311	27
228	66	256	14	284	14	312	6
229	80	257	49	285	15	313	12
230	60	258	10	286	3	314	9
231	52	259	11	287	22	315	12
232	56	260	29	288	10	316	7
233	57	261	28	289	17	318	6
234	41	262	22	290	9	319	1
235	39	263	7	291	20	320	8
236	63	264	13	292	3	321	5
237	56	265	17	293	15	322	2
238	47	266	9	294	9	323	3
239	35	267	11	295	10	324	4
240	12	268	19	296	5	325	4
241	14	269	62	297	7	326	5
242	8	270	29	298	8	327	5
243	18	271	62	299	29	328	6
244	17	272	19	300	13	329	4
245	13	273	33	301	21	330	8
246	18	274	29	302	7	331	5
247	18	275	30	303	10	332	10
248	12	276	8	304	4	333	5
249	14	277	13	305	6	334	6
250	27	278	6	306	12	335	5
251	27	279	13	307	30	336	6
252	18	280	7	308	4	337	2

Serpentine analysis Bit plane 4 Combined runs
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
338	5	367	5	396	6	424	6
339	2	368	7	397	2	425	4
340	5	369	2	398	6	426	6
341	3	370	1	399	1	427	1
342	7	371	4	400	9	428	8
343	3	372	12	401	5	429	3
344	1	374	9	402	5	430	1
345	4	375	4	403	1	431	1
346	8	376	7	404	6	432	3
347	2	377	4	405	6	434	2
348	4	378	5	406	11	435	6
349	2	379	1	407	2	436	3
350	3	380	10	408	5	437	3
351	5	381	5	409	3	438	4
352	5	382	8	410	5	439	2
353	5	383	8	411	3	440	5
354	4	384	4	412	5	441	8
355	3	385	3	413	2	442	6
356	4	386	4	414	8	443	5
357	1	387	4	415	2	444	6
358	7	388	3	416	3	445	7
359	5	389	4	417	4	446	8
360	4	390	6	418	3	447	4
362	6	391	4	419	2	448	4
363	3	392	9	420	7	449	6
364	9	393	2	421	5	450	10
365	3	394	2	422	10	451	2
366	6	395	8	423	5	452	6

Serpentine analysis Bit plane 4 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
453	2	482	6	511	3	542	2
454	2	483	2	512	7	543	2
455	1	484	15	513	5	544	1
456	7	485	3	514	6	545	1
457	6	486	7	515	2	547	1
459	8	487	5	516	6	548	3
459	1	488	6	517	2	549	1
460	6	489	5	518	4	550	1
461	1	490	15	520	1	552	3
462	13	491	2	522	5	554	2
463	1	492	5	523	5	555	3
464	4	493	4	524	5	556	2
465	5	494	9	525	3	557	2
466	5	495	1	526	7	558	2
467	3	496	7	527	1	559	4
468	7	498	3	528	8	560	2
469	6	499	5	529	1	561	2
470	5	500	3	530	8	562	2
471	4	501	2	531	1	563	3
472	3	502	1	532	4	564	1
473	2	503	3	533	3	565	1
474	9	504	8	534	4	566	6
475	4	505	1	535	3	567	3
476	9	506	11	536	2	568	1
477	2	507	5	537	3	569	2
478	14	508	7	538	3	570	4
479	1	509	5	540	3	571	3
480	7	510	6	541	3	572	6

Serpentine analysis Bit plane 4 Combined runs
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
573	3	610	2	658	1	697	1
574	2	611	1	659	1	698	2
575	1	612	2	660	1	700	2
576	1	614	2	663	2	701	1
578	4	615	3	664	2	702	1
579	1	616	2	665	4	704	1
580	3	617	3	666	3	710	1
581	3	619	1	667	1	711	2
582	4	622	1	668	2	712	3
583	4	624	2	669	1	713	5
585	3	627	2	672	1	716	2
587	1	630	2	674	1	717	2
588	7	634	1	675	1	718	1
589	1	635	2	676	2	720	1
590	2	636	1	678	2	721	1
591	1	637	1	679	1	723	1
593	1	639	1	680	1	724	1
594	2	641	1	681	2	725	1
595	2	642	1	683	1	727	4
597	2	643	2	685	1	729	1
599	2	644	3	686	1	733	1
600	1	645	1	688	1	734	2
602	2	648	1	690	1	738	1
604	1	650	4	692	1	739	2
605	5	651	1	693	1	740	2
606	3	652	1	694	2	742	1
607	4	655	2	695	1	745	1
609	1	656	1	696	2	746	2

Serpentine analysis Bit plane 4 Combined runs
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
747	1	789	1	834	1	897	1
749	1	790	1	835	1	899	1
750	1	791	2	836	1	901	1
752	1	793	1	840	2	904	1
753	1	794	1	841	2	905	1
754	1	795	1	843	2	907	1
755	1	796	1	844	1	910	1
756	2	798	1	845	1	911	2
757	1	801	1	846	2	912	2
759	2	802	1	847	3	915	2
759	2	803	1	848	1	918	2
764	1	804	1	850	3	919	1
765	2	806	1	851	2	920	1
766	3	811	1	852	1	923	1
768	1	812	1	855	1	925	1
772	1	813	2	856	1	927	2
773	1	814	1	860	3	930	2
775	2	815	4	865	1	937	2
776	1	817	2	866	1	939	3
777	1	818	1	867	1	940	2
778	1	819	1	870	1	942	1
779	3	822	2	871	1	943	2
780	1	824	1	880	1	945	3
784	1	825	2	883	2	946	3
785	1	827	1	885	1	949	1
786	1	829	1	886	1	953	2
787	1	832	1	888	1	955	1
788	1	833	1	891	2	956	5

Serpentine analysis Bit plane 4 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
959	2	994	1	1024	2	1057	7
961	2	995	3	1025	4	1059	8
963	2	996	1	1026	3	1061	4
964	1	997	1	1027	12	1063	4
965	3	998	3	1029	2	1065	6
966	2	999	3	1030	2	1067	3
967	1	1000	2	1031	2	1069	2
968	2	1001	1	1033	3	1070	3
970	1	1002	2	1034	2	1071	2
973	1	1003	4	1035	4	1072	1
974	2	1004	4	1036	1	1073	2
975	1	1005	4	1037	5	1074	1
976	1	1006	2	1038	1	1075	2
977	3	1007	5	1039	6	1076	1
978	2	1009	3	1040	1	1077	4
980	1	1010	1	1041	3	1078	3
981	2	1011	7	1042	3	1079	1
983	4	1012	1	1043	6	1080	1
984	1	1013	1	1044	1	1081	1
985	2	1015	3	1045	3	1082	4
986	3	1016	2	1046	1	1083	7
987	5	1017	2	1047	1	1085	5
988	1	1018	1	1049	5	1087	1
989	1	1019	2	1051	2	1089	2
990	1	1020	3	1052	2	1091	1
991	3	1021	5	1053	3	1092	5
992	1	1022	2	1055	7	1093	3
993	3	1023	1	1056	2	1094	1

Serpentine analysis Bit plane 4 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
1095	1	1141	2	1183	1		
1097	3	1142	3	1184	1		
1099	4	1143	1	1185	2		
1101	2	1145	3	1187	2		
1103	2	1147	4	1188	1		
1105	1	1149	5	1190	1		
1107	3	1151	3	1191	1		
1111	3	1152	1	1199	2		
1112	1	1154	2	1201	1		
1113	2	1155	3	1202	1		
1114	3	1157	1	1204	1		
1115	2	1159	1	1210	1		
1117	1	1160	1	1215	1		
1118	1	1161	3	1221	1		
1119	1	1162	2	1277	1		
1120	2	1163	2				
1121	1	1164	1				
1123	3	1165	2				
1124	3	1169	2				
1127	2	1172	1				
1129	1	1173	7				
1131	1	1174	1				
1132	1	1175	3				
1133	4	1176	2				
1135	1	1177	1				
1137	2	1179	2				
1139	1	1181	3				
1140	2	1182	2				

Serpentine analysis Bit plane 4 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
1	76351	29	513	57	63	85	7
2	28584	30	459	58	30	86	7
3	17040	31	461	59	48	87	19
4	9319	32	387	60	24	88	11
5	7102	33	373	61	50	89	17
6	5541	34	279	62	14	90	16
7	5127	35	276	63	28	91	21
8	3844	36	192	64	7	92	12
9	3695	37	212	65	23	93	21
10	2905	38	129	66	9	94	22
11	3358	39	115	67	28	95	29
12	3721	40	62	68	27	96	17
13	2633	41	58	69	41	97	25
14	1665	42	23	70	42	98	9
15	1490	43	58	71	44	99	11
16	1067	44	17	72	36	100	7
17	980	45	62	73	41	101	9
18	592	46	48	74	34	102	2
19	474	47	76	75	44	103	4
20	263	48	51	76	42	104	3
21	779	49	73	77	36	105	5
22	796	50	68	78	23	106	3
23	1173	51	99	79	22	107	5
24	119	52	63	80	16	108	6
25	318	53	76	81	17	109	12
26	541	54	66	82	9	110	8
27	632	55	89	83	4	111	14
28	545	56	73	84	5	112	9

Serpentine analysis Bit plane 5 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
STRAIGHT RLS - BINARY - STATS FILE 2 - 10/13/77

LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
113	15	141	6	170	4	199	5
114	18	142	4	171	10	200	3
115	28	143	6	172	6	201	4
116	23	144	4	173	7	202	4
117	23	145	1	174	3	203	2
118	17	146	1	175	7	204	5
119	18	147	3	176	3	205	2
120	15	148	7	177	9	206	2
121	6	149	5	178	5	207	5
122	8	150	15	179	3	208	3
123	5	151	7	180	6	209	9
124	6	152	11	181	1	210	4
125	7	153	9	182	1	211	6
126	7	154	11	183	2	212	2
127	4	155	13	184	3	213	5
128	2	156	7	186	2	214	6
129	5	157	9	187	4	215	5
130	9	158	16	188	2	216	7
131	16	159	9	189	5	217	6
132	11	160	7	190	3	218	3
133	12	161	5	191	6	219	2
134	17	162	2	192	3	220	3
135	16	163	2	193	1	222	2
136	11	164	3	194	4	223	2
137	6	165	3	195	7	224	1
138	8	167	8	196	3	225	5
139	13	168	3	197	5	226	17
140	5	169	5	198	2	227	38

Serpentine analysis Bit plane 5 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
229	51	256	13	284	1	314	19
229	62	257	5	285	1	315	17
230	38	258	2	286	1	316	4
231	45	259	1	287	2	317	5
232	71	260	5	288	8	318	9
233	51	261	20	289	5	319	5
234	28	262	3	290	6	320	13
235	38	263	3	291	1	321	17
236	50	264	2	292	7	322	18
237	61	265	2	293	14	323	14
238	27	266	4	294	6	324	6
239	10	267	2	295	8	325	9
240	3	268	4	296	23	326	3
241	8	269	2	297	7	327	6
242	19	270	9	298	3	328	8
243	2	271	4	299	2	329	2
244	1	272	9	300	14	330	3
245	1	273	11	302	2	331	11
246	4	274	7	303	8	332	11
247	8	275	9	304	5	333	6
248	3	276	4	305	4	334	10
249	4	277	11	307	2	335	8
250	12	278	4	308	1	336	6
251	7	279	2	309	43	337	6
252	9	280	8	310	13	338	14
253	6	281	5	311	3	339	13
254	3	282	4	312	6	340	6
255	6	283	3	313	15	341	4

Serpentine analysis Bit plane 5 Combined runs
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
342	4	370	2	398	12	427	5
343	7	371	7	399	7	428	2
344	2	372	4	400	4	429	1
345	5	373	2	401	2	430	1
346	2	374	1	402	1	431	3
347	14	375	6	403	7	432	2
348	7	376	9	404	7	433	4
349	1	377	6	405	4	434	3
350	2	378	5	406	4	435	3
351	8	379	31	407	2	436	7
352	9	380	6	408	4	437	3
353	5	381	2	409	7	438	3
354	14	382	10	411	4	439	8
355	26	383	11	412	3	440	4
356	10	384	6	413	3	441	2
357	15	385	7	414	3	442	1
358	12	386	6	415	2	443	18
359	22	387	3	416	2	444	13
360	20	388	4	417	3	445	5
361	15	389	4	418	20	446	2
362	12	390	7	419	3	447	1
363	15	391	6	420	2	449	3
364	23	392	1	421	6	450	2
365	3	393	4	422	8	451	1
366	4	394	2	423	11	452	1
367	7	395	4	424	8	453	2
368	10	396	3	425	18	454	1
369	9	397	19	426	29	455	5

Serpentine analysis Bit plane 5 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
456	3	484	3	518	3	552	1
457	8	485	4	519	2	555	5
458	4	486	3	520	2	556	3
459	1	487	6	521	3	557	3
460	7	488	1	522	2	558	8
461	1	489	10	523	3	559	2
462	7	490	2	524	2	560	1
463	1	491	5	527	2	561	1
464	2	492	5	528	5	563	1
465	13	493	3	529	1	564	10
466	4	495	13	531	4	565	3
467	9	496	4	532	1	566	8
468	5	497	5	534	1	567	4
469	3	498	6	535	3	568	9
470	3	499	18	536	3	569	2
471	11	500	9	537	3	570	7
472	7	501	14	538	1	571	1
473	3	502	4	539	2	573	1
474	1	503	10	540	4	574	1
475	2	504	8	541	2	575	3
476	6	506	1	542	1	576	1
477	4	508	2	543	2	578	5
478	4	509	1	544	2	580	1
479	13	510	1	546	1	581	1
480	6	511	5	547	2	583	1
481	4	513	1	548	5	586	1
482	4	516	2	549	4	587	3
483	14	517	8	550	3	588	4

Serpentine analysis Bit plane 5 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
589	1	625	4	666	2	701	1
590	1	626	2	668	5	702	1
592	5	629	1	669	2	703	1
593	5	630	2	670	1	705	2
594	11	632	1	671	1	706	1
595	2	633	3	673	3	708	3
597	4	635	1	674	3	709	3
598	5	636	1	675	5	711	1
600	1	637	2	676	2	712	2
602	2	638	3	677	1	713	3
603	2	639	4	678	2	714	1
604	1	640	1	679	1	715	2
605	1	641	2	680	5	716	1
606	2	643	1	681	3	717	7
607	1	644	1	683	2	718	4
611	1	646	2	684	5	719	2
612	1	647	2	685	1	720	3
613	2	648	1	686	1	722	1
614	2	649	3	687	1	723	5
615	2	650	2	688	2	724	2
616	4	652	4	689	2	725	2
617	6	653	1	692	1	726	5
618	3	654	2	693	1	727	1
620	2	655	1	694	2	730	2
621	3	656	2	697	1	731	1
622	2	660	1	698	8	732	4
623	2	662	4	699	1	733	2
624	1	664	3	700	1	734	3

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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
735	7	767	5	802	2	836	2
736	4	768	4	803	2	837	1
737	4	769	9	804	1	838	1
738	3	770	12	806	1	839	2
739	2	771	1	807	1	840	2
740	4	774	8	809	1	841	2
742	5	775	13	810	6	842	2
743	9	776	17	811	4	845	1
744	3	777	3	812	3	848	1
746	4	778	4	813	1	849	1
747	3	779	8	814	2	850	2
748	4	780	14	816	2	852	5
749	3	781	3	817	5	854	1
750	8	782	1	818	4	856	2
751	2	783	1	819	3	858	4
752	5	784	1	820	7	859	2
753	9	785	3	822	2	861	2
754	13	786	3	824	4	862	5
756	1	787	2	825	1	863	1
757	2	788	2	826	14	864	1
759	8	791	2	827	4	865	1
760	3	792	2	828	13	868	2
761	1	795	1	829	1	869	3
762	2	796	1	830	2	870	1
763	2	797	12	831	1	873	2
764	4	798	8	833	4	874	1
765	10	799	1	834	7	875	2
766	12	800	5	835	1	876	2

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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
877	1	924	3	973	1	1020	2
878	1	925	1	976	3	1029	5
880	1	926	1	980	2	1030	3
881	1	927	2	981	3	1031	1
882	1	928	11	982	2	1033	1
884	2	929	1	983	1	1040	1
885	2	930	7	984	4	1042	2
886	4	932	1	987	1	1043	1
888	1	934	1	988	3	1044	1
889	1	935	1	994	4	1045	1
890	3	936	2	996	2	1048	1
891	2	938	1	1000	1	1052	1
892	3	941	2	1006	2	1059	1
896	3	943	1	1010	8	1061	1
899	1	944	2	1011	3	1062	2
900	1	946	1	1012	2	1064	1
901	1	947	1	1013	1	1067	1
906	2	948	1	1015	1	1070	1
909	1	953	1	1018	3	1073	2
910	6	954	5	1019	5	1074	1
914	3	955	1	1020	4	1076	1
915	1	956	3	1021	1	1077	1
916	1	957	2	1022	3	1080	1
919	4	964	2	1023	1	1086	1
920	2	965	1	1024	12	1098	3
921	6	966	5	1025	1	1100	2
922	7	967	2	1026	2	1102	2
923	1	972	2	1027	4	1105	1

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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
1106	1	1229	2	1439	1	1632	1
1108	1	1236	1	1481	1	1639	1
1114	1	1240	7	1492	1	1640	2
1119	1	1241	5	1495	2	1641	3
1120	4	1242	1	1502	1	1643	1
1121	2	1244	1	1513	1	1646	1
1124	2	1256	1	1514	1	1647	4
1126	1	1257	5	1528	2	1648	2
1127	2	1260	1	1537	2	1652	5
1144	3	1272	2	1546	1	1653	2
1148	1	1273	1	1554	1	1654	1
1155	1	1275	1	1557	1	1655	1
1160	1	1280	2	1560	1	1658	2
1161	1	1281	1	1564	1	1660	4
1164	1	1296	1	1586	2	1661	7
1166	1	1297	1	1598	1	1662	82
1170	1	1301	3	1603	1	1663	331
1171	1	1308	1	1604	2	1664	29
1183	2	1318	1	1605	1	1665	3
1190	1	1334	1	1606	7	1686	1
1192	1	1339	6	1607	2		
1202	1	1343	1	1614	1		
1203	1	1346	1	1617	1		
1218	1	1358	1	1623	2		
1219	2	1413	1	1625	1		
1220	2	1418	1	1628	1		
1221	1	1421	1	1629	1		
1225	1	1431	1	1630	1		

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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
1	2272	29	480	57	48	85	5
2	2835	30	448	58	30	86	7
3	15347	31	410	59	37	87	17
4	16494	32	381	60	23	88	9
5	5943	33	331	61	31	89	13
6	4949	34	269	62	10	90	16
7	4080	35	239	63	18	91	18
8	3911	36	189	64	6	92	13
9	3643	37	169	65	13	93	19
10	3632	38	119	66	8	94	22
11	3957	39	85	67	23	95	24
12	3318	40	57	68	26	96	16
13	3399	41	43	69	35	97	22
14	3033	42	20	70	42	98	7
15	1380	43	25	71	42	99	8
16	1024	44	18	72	34	100	7
17	734	45	41	73	33	101	6
18	549	46	47	74	36	102	2
19	326	47	46	75	41	103	1
20	229	48	50	76	41	104	1
21	194	49	59	77	32	105	1
22	374	50	69	78	21	106	2
23	705	51	84	79	17	107	4
24	1334	52	55	80	17	108	5
25	316	53	72	81	16	109	11
26	535	54	60	82	9	110	8
27	572	55	80	83	2	111	14
28	541	56	67	84	4	112	9

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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
113	12	141	3	171	9	200	3
114	17	142	4	172	6	201	4
115	26	143	6	173	7	202	4
116	22	144	4	174	3	203	2
117	22	146	1	175	8	204	5
118	17	147	4	176	4	205	2
119	18	148	7	177	8	206	2
120	15	149	5	178	4	207	5
121	7	150	15	179	2	208	3
122	5	151	6	180	6	209	7
123	4	152	11	181	1	210	4
124	5	153	11	182	1	211	5
125	6	154	11	183	2	212	2
126	6	155	10	184	3	213	5
127	4	156	7	186	2	214	6
128	2	157	8	187	3	215	5
129	5	158	16	188	2	216	7
130	9	159	8	189	4	217	5
131	15	160	7	190	2	218	2
132	13	161	5	191	6	219	2
133	12	162	2	192	3	220	3
134	15	163	2	193	1	222	1
135	15	164	2	194	2	223	2
136	10	165	1	195	7	224	1
137	6	167	7	196	3	225	5
138	8	168	3	197	5	226	17
139	13	169	6	198	2	227	38
140	5	170	3	199	5	228	52

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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
229	62	257	5	287	2	317	3
230	37	258	2	288	8	318	9
231	45	259	1	289	5	319	5
232	71	260	5	290	6	320	13
233	51	261	21	291	1	321	17
234	29	262	5	292	7	322	10
235	58	263	2	293	14	323	14
236	50	265	2	294	6	324	6
237	60	266	4	295	8	325	9
238	27	267	2	296	23	326	3
239	10	268	4	297	7	327	6
240	3	269	2	298	3	328	9
241	8	270	9	299	2	329	2
242	19	271	4	300	14	330	2
243	1	272	9	302	2	331	11
244	1	273	11	303	8	332	11
245	1	274	7	304	5	333	6
246	4	275	9	305	4	334	10
247	8	276	4	307	2	335	8
248	3	277	11	308	1	336	6
249	4	278	4	309	43	337	6
250	12	279	2	310	13	338	14
251	7	280	8	311	3	339	13
252	9	281	5	312	6	340	6
253	6	282	4	313	15	341	4
254	3	283	2	314	19	342	4
255	6	284	1	315	17	343	7
256	12	285	1	316	4	344	2

Serpentine analysis Bit plane 6 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
345	5	373	1	402	1	432	1
346	2	375	6	403	7	433	2
347	14	376	9	404	7	434	2
348	7	377	6	405	4	435	3
349	1	378	5	406	4	436	6
350	2	379	31	407	2	437	1
351	8	380	6	408	4	438	3
352	9	381	1	409	7	439	2
353	5	382	10	411	4	440	2
354	14	383	11	412	2	441	2
355	26	384	6	413	3	443	2
356	10	385	7	414	2	444	5
357	15	386	6	415	2	445	3
358	12	387	3	416	2	446	2
359	22	388	4	417	3	447	1
360	20	389	4	418	21	449	3
361	15	390	7	419	3	450	2
362	12	391	6	420	2	451	1
363	15	392	1	421	4	452	1
364	23	393	4	422	7	454	1
365	3	394	2	423	11	455	2
366	4	395	4	424	8	456	3
367	8	396	3	425	17	457	7
368	10	397	19	426	29	458	4
369	5	398	13	427	5	459	1
370	2	399	7	428	1	460	5
371	7	400	3	429	1	461	1
372	4	401	2	430	1	462	3

Serpentine analysis Bit plane 6 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
464	2	502	2	546	1	593	5
465	1	503	1	547	2	594	11
466	2	506	1	548	1	595	1
467	4	508	2	555	4	600	1
468	4	509	1	557	3	602	1
471	2	510	1	558	5	603	2
472	5	511	3	559	2	604	1
475	2	513	1	560	1	605	1
476	6	516	2	561	1	607	1
477	2	517	5	563	1	611	1
478	1	518	2	564	1	613	2
479	2	519	2	565	1	614	1
480	3	520	2	566	1	615	1
481	2	521	3	567	4	616	1
482	3	522	2	568	2	617	6
483	3	523	2	570	5	620	2
484	1	524	1	571	1	621	3
485	3	527	1	573	1	622	1
486	2	528	3	574	1	623	2
487	1	529	1	575	2	624	1
491	1	531	4	576	1	625	4
495	1	535	1	578	2	626	2
496	3	536	2	581	1	629	1
497	3	537	3	587	3	630	1
498	5	539	2	588	4	632	1
499	10	540	4	589	1	633	3
500	6	541	2	590	1	635	1
501	5	542	1	592	4	637	2

Serpentine analysis Bit plane 6 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
638	3	685	1	733	1	795	1
639	4	686	1	734	1	796	1
640	1	689	2	735	5	797	7
641	2	693	1	736	4	798	3
643	1	697	1	737	1	799	1
644	1	698	3	738	1	800	3
645	1	699	1	739	1	802	1
646	2	700	1	740	2	803	2
647	2	701	1	742	3	804	1
649	2	702	1	744	2	806	1
649	1	705	2	746	3	810	3
650	1	706	1	747	1	811	2
655	1	708	1	748	2	812	1
660	1	709	3	750	1	816	1
662	4	711	1	752	1	817	3
664	3	712	2	754	1	819	1
666	2	713	3	756	1	822	2
668	1	714	1	757	2	827	3
671	1	715	1	759	4	828	2
673	3	716	1	762	1	829	1
674	2	717	6	770	1	835	1
675	5	718	1	776	3	836	1
676	2	719	1	777	2	837	1
677	1	720	1	778	3	838	1
679	1	726	4	783	1	839	1
680	5	730	2	785	1	841	1
681	3	731	1	786	1	842	1
684	2	732	2	792	2	844	1

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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
849	1	914	3	964	1	1020	2
849	1	915	1	965	1	1029	5
850	2	919	4	966	5	1030	3
852	1	920	2	967	1	1031	1
856	1	921	6	972	1	1033	1
858	3	922	6	981	1	1035	2
859	1	923	2	982	2	1042	2
861	2	924	3	983	1	1043	1
862	5	925	1	984	1	1045	1
863	1	926	1	987	1	1057	1
864	1	927	2	988	1	1058	1
865	1	928	10	992	1	1059	1
868	2	929	1	1010	2	1061	1
869	3	930	3	1011	2	1062	2
870	1	932	1	1012	6	1064	1
874	1	934	1	1013	19	1067	1
875	1	935	1	1014	21	1070	2
877	1	936	1	1015	24	1073	2
878	1	938	1	1018	1	1074	2
881	1	941	2	1019	3	1077	1
882	1	943	1	1020	4	1080	1
884	1	944	1	1021	1	1098	1
886	1	946	1	1022	2	1100	2
889	1	947	1	1023	1	1102	2
891	1	948	1	1024	12	1105	1
899	1	955	1	1025	2	1116	1
909	1	956	1	1026	2	1119	2
910	1	957	1	1027	4	1120	4

Serpentine analysis Bit plane 6 Combined runs
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LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE	LENGTH	VALUE
1131	2	1257	5	1502	1	1639	1
1143	1	1260	1	1513	1	1640	2
1144	2	1272	2	1514	1	1641	3
1146	1	1273	1	1528	2	1642	1
1148	1	1274	1	1537	3	1643	1
1155	1	1275	1	1538	1	1646	1
1161	1	1280	2	1546	1	1647	5
1164	1	1281	1	1554	1	1648	2
1166	1	1296	1	1557	1	1652	5
1170	1	1297	1	1560	1	1653	3
1171	1	1301	4	1564	1	1654	1
1180	1	1308	1	1586	2	1655	1
1183	2	1318	1	1591	1	1658	2
1190	1	1334	1	1598	1	1660	6
1197	1	1339	6	1599	1	1661	8
1202	1	1343	1	1603	2	1662	82
1218	1	1346	1	1604	2	1663	474
1219	2	1358	1	1605	1	1664	141
1220	2	1371	1	1606	8	1665	94
1221	1	1410	1	1607	2		
1225	1	1413	1	1614	1		
1229	2	1418	1	1617	1		
1236	1	1421	1	1623	2		
1240	7	1431	1	1625	1		
1241	5	1439	1	1628	2		
1242	1	1481	1	1629	1		
1244	1	1492	1	1630	1		
1256	1	1495	2	1632	1		

Serpentine analysis Bit plane 6 Combined runs
TYPED PAGE - PRESCAN - UNCORRECTED - NOSC #34 FILE 1
STRAIGHT RLS - BINARY - STATS FILE 2 - 10/13/77

ANNEX B: "QUICK-FAX" PRESENTATION

DIGITAL FACSIMILE EQUIPMENT " Quick- FAX" USING A NEW REDUNDANCY REDUCTION TECHNIQUE

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DIGITAL FACSIMILE EQUIPMENT "Quick-FAX" USING A NEW REDUNDANCY REDUCTION TECHNIQUE

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ABSTRACT

In the field of facsimile communications, one of the most important technical problems is to attain the shortening of the transmission time to the extent possible. To cope with this requirement, a new technique of redundancy reduction for facsimile signals is introduced.

In this paper, the principle of the Relative Address Coding (RAC) which is characterized by its remarkable reduction of redundant information is presented, as well as the development of a digital facsimile equipment applying the technique. RAC method is so effective in redundancy reduction that the compression factor is approximately 3.3 ~ 1.1 times as large as that of the conventional Run Length Coding.

Quick-FAX, high-speed digital facsimile equipment, has been developed to confirm the effectiveness of RAC method. In order to ensure the reliable communication, transmission procedure of Quick-FAX is based on the High level Data Link Control (HDLC) procedure for data communications. As the test result of Quick-FAX, an A-4 size document is transmitted in about 30 seconds at the transmission rate of 4800 bps.

1. INTRODUCTION

The recent progress of electronic technology and the development of worldwide telecommunication networks make it possible to offer various new communication services. The demands for the facsimile service, by which various documents and drawings can be reproduced at the remote ends exactly and rapidly with simple operation, are remarkably increasing in these years.

One of the most important technical problems in facsimile communications is to attain the shortening of the transmission time to the extent possible. To cope with this requirement, studies[1] have been made at the Laboratories of KDD relating to a new technique of redundancy reduction for facsimile signals.

In this paper, the principle of the Relative Address Coding (RAC) which is characterized by its remarkable reduction of redundant information is presented, as well as the development of a digital facsimile equipment applying the technique. RAC method has specific features of facsimile coding, where the characteristics of crosscorrelation between adjacent scanning lines are fully utilized as well as that of autocorrelation on each scanning line. The compression factor is approximately 3.3 ~ 1.1 times as large as that of the conventional Run Length Coding.

Quick-FAX, high-speed digital facsimile equipment, has been developed to confirm the effectiveness of RAC method in the laboratory test. Considering that the digital facsimile has commonality with data communication, transmission procedure of Quick-FAX is based on the High level Data Link Control (HDLC) procedure.

In order to ensure the reliable operation, those control signals such as Command and Response received incorrectly are corrected automatically by means of retransmission procedure. And as for the facsimile information transfer phase, the retransmission technique is not adopted to avoid the inefficient transmission caused by the time-consuming procedure for the acknowledgement of reception. Instead, in order to maintain the legibility of reproduced copy, such processings as prevention of error propagation in the copy and replacement of mutilated scanning line by the predecessor are adopted.

As the test results of Quick-FAX, it is concluded an A-4 size document is transmitted in about 30 seconds at the transmission rate of 4800 bps.

2. RELATIVE ADDRESS CODING FOR FACSIMILE SIGNALS

2.1 Transition Elements

The facsimile signals obtained by scanning the document comprise black and white picture elements as shown in Fig. 1. In order to reproduce the copy of the original document at the receiving end, it is sufficient to encode and transmit the addresses of only transition elements, which are defined as those picture elements whose information has changed from black to white or vice versa. The picture elements P, P', Q, Q', R and R' in Fig. 1 are transition elements.

Transition elements can be classified into 3 kinds as shown in Fig. 2.

(i) STH: Starting Transition element of Head run: An STH is the first picture element of a head run. Here, a head run is such a black or white run that there exists no picture elements on the preceding line, which are of the same colour and adjacent to the run.

(ii) ETH: Ending Transition element of Head run: An ETH is the transition element next to the head run.

(iii) DTE: Displacement Transition Element; A DTE is the transition element which is not STH nor ETH.

The address of an STH depends on the position where the character or the figure is described, and the address of an ETH depends on the length of the head run. The address of a DTE is dependent on the length of displacement.

The total number of transition elements may indicate the amount of information in the document, and the ratio of the number of STH and ETH to the total number of transition elements may indicate the complexity of the document.

In the conventional Run Length Coding (RLC), the address of every kind of transition element is represented by the distance from the preceding transition element in terms of the number of picture elements[2], making good use of the statistical intra-line correlation. The facsimile signals,

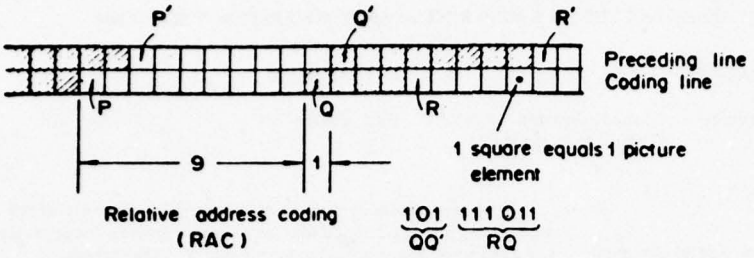

Fig.1 Principle of Relative Address Coding (RAC)

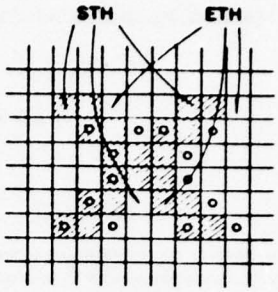

Fig.2 Example of transition elements

however, have the inter-line correlation as well as the intra-line correlation.[3]

The address of a transition element can be represented by the distance from any transition element where address is already encoded and transmitted. The address of a DTE is to be encoded, making use of the length of displacement, the distance from the transition element on the preceding line. The addresses of STH and ETH are to be encoded making use of the distance from the preceding transition element on the same line.

Table 1 shows an example of the numbers of three kinds of transition elements. As is easily expected, DTE is dominant and its probability of expectation is generally more than 80%. The probability of expectation of STH or ETH is generally less than 10%. Hence, it is important to take into account this partiality of probability and to assign efficient codes to DTE especially.

Table 1 Example of the numbers of STH, ETH and DTE (Document of Japanese character with the resolution of 5×5 pel/mm)

Transition Element	Number	Probability (%)
STH	36,225	86.7
ETH	2,776	6.6
DTE	2,776	6.6
Total	41,777	100.0

2.2 Principle of RAC Method

The Relative Address Coding[4] (RAC) for facsimile signals makes good use of both inter-line and intra-line correlations, and is easy to implement because of no strict classification of transition elements.

The principle of RAC is explained, taking an example of encoding the transition element Q in Fig. 1. In regard to the transition element Q, two reference elements are selected according to the following rule among the transition elements that are already encoded.

(i) The first reference element P is the preceding transition element on the same line to the transition element Q. In the case that the first reference element above defined does not exist, the first picture element on the line is to be the first reference element.

(ii) The second reference element Q' is the transition element that has the same direction of transition as the transition element Q and is the nearest to the first reference element P on its right side. In the case that the element above defined does not exist, the second reference element is the imaginary picture element next to the last picture element on the preceding line.

The address of transition element Q is encoded by the distance from the standard element that is selected between the two reference elements P and Q'. In the case that the distance from the first reference element P to the transition element Q is more than 1 (Picture element) and that the first reference element P is nearer to Q than the second reference element Q', the first reference element P is selected to be the standard element, and the distance is expressed by the number without sign. In all other cases, the second reference element Q' is selected to be the standard element, and the distance from Q' to Q is expressed by the number with + or − sign according to the direction. (Table 2) For each distance, variable length code shown in Table 3 is assigned.

Table 2 The signs used in RAC

Position of the reference element in relation to the transition element	Sign
On the SAME line	No sign
On the PRECEDING line, JUST UPON or LEFT	+
On the PRECEDING line, RIGHT	−

The most efficient code is a well-known Huffman's code[5], but it needs a great capacity of memory to implement the code. Codes shown in Table 3 are defined from the statistics of distribution of every distance to be coded, which are obtained by computer simulation.

The distinctive feature of Table 3 is the few bits assigned to the distances "+0", "+1" and "-1", which results from the fact that the probabilities of expectation of such distance are very much larger than those of the other distances.

For example, in case of coding the transition element Q in Fig. 1, since the distance PQ (=9) is greater than the distance QQ' (=1), Q' is selected to be the standard element. As the standard element Q' is on the right of the transition element Q, the address of Q is encoded by the distance QQ' with a "−" sign, that is "-1", which is coded as "101" according to Table 3.

As mentioned above, in RAC method only the addresses of transition elements are sequentially encoded, making use of the distance, that is, the relative address from the transition element mostly on the preceding line.

Table 3 Code used in RAC
(a) Assignment of codes for the distances
(b) Assignment of supplementary codes to (a)

(a)

Distance	Code
+0	0
+1	100
-1	101
N (N≧1)	111 F (N)
+N (N≧2)	1100 F (N-1)
-N (N≧2)	1101 F (N-1)

(b)

N	F (N)
1 ~ 4	0••
5 ~ 20	10••••
21 ~ 84	110••••••
85 ~ 340	1110••••••••
341 ~ 1364	11110••••••••••
1365 ~ 5460	111110••••••••••••

2.3 Computer Simulation Results of RAC Method

There have already been proposed many data compression methods for high-speed facsimile transmission, some of which are proposed to the standard coding method at CCITT SG XIV. Eight test documents were specified at the Rapporteurs meeting held at Geneva in 1975.

Computer simulation of RAC method for the 8 test documents has been made in the two cases with the resolution of 8 pel (picture element) / mm and 4 pel/mm in both horizontal and vertical directions. From computer simulation it is clear that the standard element is selected from the second reference element with the probability of 0.80 to 0.95, which means most of the transition elements in RAC are encoded by the distance from the transition element on the preceding line.

Fig. 3 shows the probability distribution of the distance coded for the test document #1 (English letter) with the resolution of 8 pel/mm in both directions. The solid line and the dot-dash-line correspond to the distance from the second reference element to the transition element to be coded and the broken line corresponds to the distance from the first reference element. The dotted line is the distribution of run-length in RLC for reference.

All the distribution curves of RAC are generally exponential and the probabilities for the distance "+0", "+1" and "-1" are approximately 0.5, 0.13 and 0.13 respectively. For such short distances with large probability assigned are few bit codes, as suggested in 2.2. The change of resolution results in very little change in the distribution curve of RAC.

On the other hand, the distribution of RLC increases in according as the run-length increases from 1 to 4 and is also exponential in the range of the run-length longer than 4. The distribution of RLC changes its curve to short run-length, though it is not so distinctive, according to the decrease of resolution.

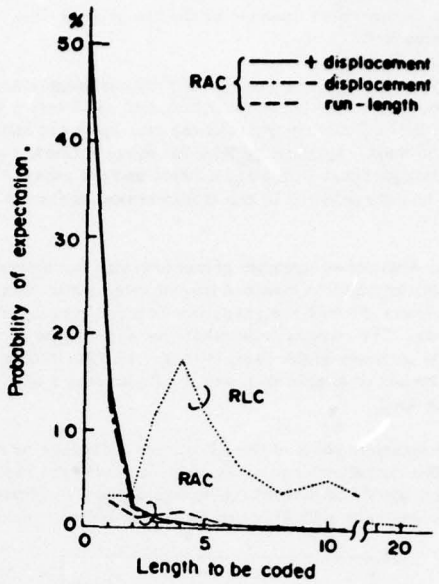

Fig.3 Distribution of Length to be coded
Test document # 1, Resolution: 8×8 pel /mm

The difference between the distribution of RAC and that of RLC is the concentration of probability on the short distances of RAC. This means the amount of information in RAC is less than that in RLC according to the information theory.

In Table 4, shown are the compression factors of RAC and RLC, which are defined as the number of total picture elements divided by the number of bits encoded. In RAC method, codes shown in Table 3 are used and in RLC only F(N) in Table 3 is used from run-length 1. From the result of Table 4, it is concluded that the compression factor of RAC is 330% ~ 110% larger than that of RLC.

Table 4 Compression factor

Res.	Coding / Doc.	1	2	3	4	5	6	7	8
8 × 8	RAC	28.0	48.9	18.2	7.1	16.1	30.0	7.3	27.0
	RLC	12.9	14.9	7.6	4.3	7.2	9.6	4.3	8.6
4 × 4	RAC	13.7	24.5	9.1	3.5	7.9	15.8	3.6	13.5
	RLC	9.0	9.2	5.3	3.16	5.03	6.49	3.05	5.4

2.4 Control of Error Propagation

In this section the effect of transmission errors is investigated and the method of controlling the error propagation is presented.

In RAC method, most of the transition elements are encoded by the distance from the elements on the preceding line. Once an error occurs on coded signals, then it results in the change of the address of the transition element in question and in many cases also in the change of the addresses of most of the transition elements after the transition element in question. This error propagation phe-

nomenon is inevitable because of the use of inter-line correlation in RAC.

In order to stop and control the error propagation, mixing of RAC with RLC is proposed, that is, every k lines is coded by RLC method whereas the rest lines are coded by RAC method. By adopting RLC for every k lines, the error propagation is limited to k lines, and the average number of lines affected by the transmission error is (k+1)/2.

Fig. 4 shows an example of compression factor versus Parameter k, which is obtained by computer simulation for test document #1 with the resolution of 8 pel/mm in both directions. The compression factor becomes large according to the increase of the Parameter k. The Parameter k of 1 corresponds to simple RLC and the Parameter k of ∞ to complete RAC.

The optimum value of the Parameter k depends on the size of the characters on the document and also the resolution and it should be defined taking into account the legibility of the document with affection by transmission errors.

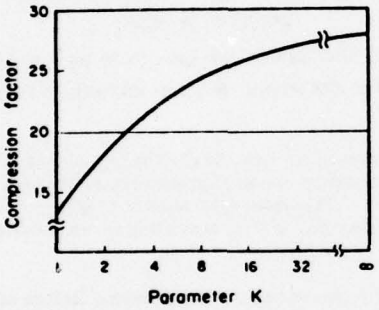

Fig. 4 Compression factor versus Parameter K
Test document #1, Resolution : 8x8 pel/mm

3. DIGITAL FACSIMILE EQUIPMENT "Quick-FAX"

A digital facsimile equipment, to which Relative Address Coding (RAC) method is adopted to reduce the redundancy of facsimile signals, has been built as a prototype model and named "Quick-FAX".[6] The specific feature of Quick-FAX is that it has the capability of high-speed transmission by RAC method and the commonality with data transmission.

3.1 Performance of Quick-FAX

The transmitter and receiver of Quick-FAX is shown in Photo. 1 and the specifications are summarized in Table 5. According to the fineness of letters and lines in the documents, the resolution is to be selected 4 or 8 pel/mm in horizontal and vertical directions. The scanning speed is controlled by the stepping motor at 200 line/second maximum. These scanned facsimile signals are coded by Relative Address Coding (RAC) and sent in frame configuration through 4800 bps MODEM (CCITT V27). Up to about 30 sheets of document can be automatically transmitted with only the initial operation.

At the receiver, every operation to start or stop the equipment and to set the resolution is automatically performed and therefore the receiver has the facility of unattended reception. The recording method is electrostatic with multistylus. In the case of the resolution of 4 pel/mm in the horizontal direction, every two picture elements, whose information is not transmitted, is filled up with the same information as the preceding picture element. In case of the resolution of 4 line/mm in the vertical direction, the information of the lines omitted at the transmitter are interpolated with the information of the preceding line.

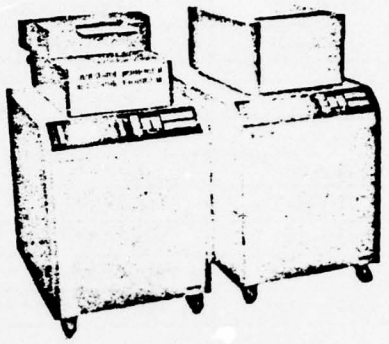

Photo. 1 Transmitter (left) and receiver (right) of Quick - FAX

Table 5 Specifications of Quick-FAX

Page size	ISO A4 (210 mm × 297 mm)
Resolution	Horiz. 4/8 pel/mm (changeable) Vert. 4/8 pel/mm (changeable)
Scanning	Flat bed with photo diode array
Line scanning speed	200 lines/sec
Recording	Electrostatic
Data compression	RAC (Relative Address Coding)
Transmission rate	4,800 bit/sec
Modulation	8-phase differential PSK
Link control	Modified HDLC
Facilities	Automatic continuous loading (Up to 30 documents) Unattended reception
Control for the erroneous line	Replacing by the predecessor or white line

3.2 Data Link Control

Considering that the digital facsimile has close resemblance to data communication, it is desirable that digital facsimile signals are transmitted in the same manner as data information.

The high level data link control (HDLC) procedure, which is to be standardized in ISO, has several convenient features such as variable frame length, frame sequence control by double numbering, error control by cyclic redundancy check code and bit transparency by "0" insertion.

The transmission procedure of Quick-FAX is based on HDLC and the frame structure is almost the same as HDLC as shown in Fig. 5. Though Address field is allocated between Flag and Control Field in HDLC, it is omitted in

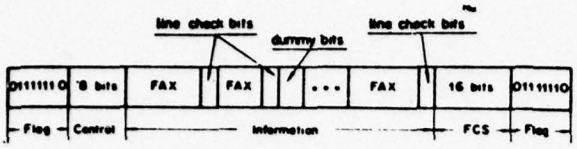

Fig.5 Frame structure

Quick-FAX because it is not necessary for point to point communication. The signals particular to facsimile communication, such as the control signals to start or stop the remote equipment and to set the resolution, are newly defined as coded signals and allocated in Control field and, if necessary, in Information field.

The coded facsimile signals are transmitted in Information field. The number of lines included in a frame can be set to 4, 8 or all the lines in the document. The signals of the first line in each frame are coded by the conventional run length coding whose code assignment is the same as F(N) in Table 3.

After facsimile signals of a line are coded, the number of the bits to be set "1" in the coded signals of the line are counted with modulus 8 and the least significant 3 bits of the result are inverted and added as line check bits to the coded facsimile signals. Moreover in the case that the number of coded signals of each line is less than 24 (corresponds 5 ms at a rate of 4800 bps), the dummy bits are attached to the coded facsimile signals in order to guarantee the recording time (5 ms) of the line at the receiver.

As described above, all the control signals and the coded facsimile signals, together with the Flag (8 bits), FCS (16 bits), line check bits (3 bits) and dummy bits, are transmitted in frame configuration through 4800 bps MODEM. Though the transmission time depends on the amount of information in a document, Quick-FAX can transmit the typical Japanese character test document with the resolution of 4 pel/mm in both horizontal and vertical directions within about 24 seconds.

3.3 Error Control

The control signals which control the remote equipment are so important that each frame including the control signals is sent after confirming the response of the preceding control signal. At the receiver, control frame received is checked by frame check sequence (FCS), and if the frame is not received correctly, the receiver sends no response. At the transmitter, if the response to a control signal cannot be received within a predetermined interval, the same control signal is retransmitted (three times at most).

On the other hand, the information frames which include the coded facsimile signals, line check bits and dummy bits in Information field are continuously transmitted without confirming the response. At the receiver, whenever signals of each line are decoded, they are checked by the line check bits. If transmission errors are detected in a line, the correct signals of the preceding line are repeated instead of the erroneous line and the rest signals in the frame are all discarded. Thereby the affection of a transmission error never propagates beyond the frame since the facsimile signals of the first line in each frame is coded by run length coding independently of the signals in the preceding frame.

Transmission test has been performed under the error generating condition which is specified at the Rapporteurs Meeting in CCITT SG XIV. The result of the test indicates that the legibility of the reproduced copy is satisfactorily maintained against transmission errors in the case that a frame includes coded signals of 4 lines.

4. CONCLUSION

The principle and theoretical investigation of a new two-dimensional coding method RAC have been presented in this article, as well as the development of high-speed digital facsimile equipment "Quick-FAX" by use of this technique.

From the test result, it has been proved that RAC method is so effective that an A-4 size document is transmitted in about 30 seconds at the transmission rate of 4800 bps. At the Special Rapporteurs Meeting of CCITT SG. XIV (Facsimile) in 1975, RAC method was evaluated to be the most efficient method with respect to the compression factor among principal redundancy reduction techniques proposed to the Study Group.

Quick-FAX has been developed for the purpose of realization of RAC method, where a new data link control procedure was adopted to ensure the commonality with data communications.

The digital facsimile which has such specific features as time-saving transmission and high quality reception is expected to be used extensively and to play an important role in telecommunications, together with the progress of electronic technology and the development of digital networks.

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